1 Introduction

Freescale provides the M74K mask sets of the 9S08DZ60 to address a number of errata found on previous mask sets, including errata associated with the timer PWM module (TPM) module.

Both the 0M74K and 1M74K mask sets may be offered to customers. There are no functional differences between the 0M74K and 1M74K. The remainder of the document will refer to the M74K to denote both.

This document addresses the differences between the two mask sets, 3M05C and M74K. This application note does not describe in detail how to use the DZ60 in a particular system. It highlights the differences from the earlier mask set versions and provides guidance in migrating code. Programmers and designers must consult the specific HCS08 MCU data sheet for further information on using and programming the device. This application note also refers to errata data PWM Boundary Case Issues in HCS08 Timer PWM Module (TPM).
Introducing the DZ60 and the M74K Mask set.

SE110-TPM. To download this document go to freescale.com

Device mask sets can be identified by the part markings that include the mask set on the device package.

NOTE
With the exception of mask set errata documents, if any other Freescale document contains information that conflicts with the information in the device data sheet, the data sheet must be considered to have the most current and correct data.

The major differences between the 3M05C and M74K mask sets are within the following modules:

- Multi-purpose clock generator (MCG)
- Timer / pulse width modulation (TPM)
- Inter-integrated circuit (IIC) serial peripheral
- EEPROM
- Port pin, PTA7
- MSCAN

2 Introducing the DZ60 and the M74K Mask set.

Further expanding the core’s offerings in the automotive and industrial spaces by adding CAN and EEPROM, the DZ60 represents an evolutionary step for Freescale’s S08 family.

The M74K mask set addresses errata and CAN bus conformance issues can seen in the 3M05C mask set DZ60 to better support those application spaces.

2.1 M74K 9S08DZ60 Enhanced Features Over the 3M05C Version

Multi-purpose clock generator (MCG)
- Addressed narrow clock pulse errata, sometimes encountered in FEI/FEE mode

Timer/pulse width modulation (TPMv3)
- Addressed errata. See *PWM Boundary Case Issues in HCS08 Timer PWM Module (TPM)* SE110-TPM found in TPM v2

Inter-integrated circuit (IIC) serial peripheral
- 10-bit operation is now available

NOTE
High drive strength setting on ports still prohibits IIC functionality.

EEPROM — Blank check correctly shows state of EEPROM locations
PTA7/ADP7 — Able to use the ADC channel AD7
MSCAN — Conformance robustness issue fixed
3 Multi-Purpose Clock Generator (MCG)

The M74K addresses an errata sometimes observed when the FLL is enabled where the output of the MCG has short clock pulses that potentially lead to runaway code. There are no functional differences between the 3M05C and M74K other than eliminating the errata behavior. No code considerations are necessary.

4 Timer PWM Module v3

The M74K timer module is essentially the same on the 3M05C. The way the timer modules have been integrated into the MCU is slightly different. These differences can be summarized as:

- TPMxCnVH:TPMxCnVL latching
- Coherency mechanism in background debug mode

In the process of addressing some errata associated with the TPMv2, necessary design changes were made that have impacted behavior in a few modes. These module changes were implemented to address TPM functional shortcomings for using in a number of targeted applications. These changes also maintain compatibility with newer S08 devices.

As a result, the order that registers are written to configure the TPM modules may vary from TPMv2 to TPMv3.

5 TPMxCnVH:TPMxCnVL Latching

On the M74K the latching mechanism for registers TPMxCnVH:TPMxCnVL is different from the 3M05C.

5.1 Input Capture Mode

In the input capture mode, reading either byte (TPMxCnVH or TPMxCnVL) latches the contents of both bytes into a buffer where they remain until the other byte is read. This is true for both the M74K and 3M05C.

On the M74K writes to TPMxCnVH:TPMxCnVL are ignored in input capture mode. On the 3M05C it is possible to write to TPMxCnVH:TPMxCnVL in input capture mode.
5.2 Output Compare Mode

In output compare mode, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer.

For the 3M05C, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value after the second byte has been written.

In the case of the M74K, the TPMxCnVH:L registers are updated from the buffer, as a coherent 16-bit value according to the value of CLKS bits.

If \((\text{CLKS}[1:0] = 00)\), the registers are then updated when the second byte is written.

If \((\text{CLKS}[1:0] 00)\), the registers are then updated at the next TPM counter change (end of the prescaler counting) after the second byte is written.

5.3 Edge Aligned PWM Mode

In the edge aligned PWM mode, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer.

For the 3M05C, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value when the TPM counter changes from TPMxMODH:L to $0000 after the second byte has been written.

In the case of the M74K, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value according to the value of CLKS bits.

If \((\text{CLKS}[1:0] = 00)\), the registers are then updated when the second byte is written.

If \((\text{CLKS}[1:0] 00)\), the registers are then updated after the second byte has been written when the TPM counter changes from \((\text{TPMxMODH:L} - 1)\) to \((\text{TPMxMODH:L})\). If the TPM counter is a free-running counter, the TPMxCnVH:L registers are then updated when the TPM counter changes from $FFFF to $FFFE.

5.4 Center Aligned PWM Mode

In center aligned PWM mode, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer.

For the 3M05C, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value when the TPM counter changes from TPMxMODH:L to \((\text{TPMxMODH:L} - 1)\) after the second byte has been written.

In the case of the M74K, the TPMxCnVH:L registers are updated from the buffer as a coherent 16-bit value according to the value of CLKS bits.

If \((\text{CLKS}[1:0] = 00)\), the registers are then updated when the second byte is written.

If \((\text{CLKS}[1:0] 00)\), the registers are then updated after the second byte has been written when the TPM counter changes from \((\text{TPMxMODH:L} - 1)\) to \((\text{TPMxMODH:L})\). If the TPM counter is a free-running counter, then the TPMxCnVH:L registers are updated when the TPM counter changes from $FFFE to $FFFF.
5.5  Resetting the Latching Mechanism

Writing to TPMxCnSC resets the latching mechanism for TPMxCnVH:L on both the 3M05C and M74K. In input capture mode writing to TPMxCnSC after reading one channel value register but before reading the other resets the latching mechanism and may result in the current channel value register data being over written if a new input capture occurs.

In output compare or PWM modes writing to TPMxCnSC, after writing to the channel value registers TPMxCnVH:L before they are updated, effectively cancels the write to TPMxCnVH:L leaving the register values unchanged.

This is particularly relevant for the M74K, depending upon the configuration of CLKS and the selected mode there could be a considerable time before registers TPMxCnVH:TPMxCnVL are updated. It is therefore important to ensure that TPMxCnSC is not written during this time unless the user wishes to cancel a previous write to the channel value registers.

As a result of these differences in the latching mechanism, users may have to initialize their timer registers in a different order than before to allow this.

6  Coherency Mechanism in Background Debug Mode (BDM)

Registers TPMxCNTH:L, TPMxMODH:L, and TPMxCnVH:L have a coherency mechanism that latches both bytes of the register into a buffer where they remain latched until both bytes have been accessed. This allows coherent 16-bit reads or writes in either big-endian or little-endian order for easier implementation.

On the M74K this coherency mechanism behaves differently from the 3M05C in background debug mode.

TPMxCNTH:L — On the M74K any read of TPMxCNTH:L registers in background debug mode returns the value of the TPM counter which is frozen.

For the 3M05C, if only one byte of the TPMxCNTH:L registers was read before entering BDM, then any subsequent read of TPMxCNTH:L registers during BDM returns the latched value of TPMxCNTH:L from the read buffer instead of the frozen TPM counter value.

On the M74K the read coherency mechanism can be reset in BDM if there is a write to TPMxSC, TPMxCNTH, or TPMxCNTL. These conditions do not reset the read coherency mechanism on the 3M05C.

TPMxCnVH:L — On the M74K any read of TPMxCnVH:L registers in background debug mode returns the value of these registers.

For the 3M05C, if only one byte of the TPMxCnVH:L registers was read before entering BDM, then any subsequent read of TPMxCnVH:L registers during BDM returns the latched value of TPMxCnVH:L from the read buffer instead of the value from the registers.

On the M74K the read coherency mechanism can be reset in BDM if there is a write to TPMxCnSC. This condition does not reset the read coherency mechanism on the 3M05C.
TPMxMODH:L — On the M74K the write coherency mechanism of the TPMxMODH:L registers can be reset in BDM if there is a write to TPMxSC. This condition does not reset the read coherency mechanism on the 3M05C.

For more information on the TPM, please refer to the Freescale document MC9S08DZ60 Data Sheet.

7 Inter-Integrated Circuit (IIC)

The inter-integrated circuit (IIC) peripheral on the M74K offers all the functionality of the 3M05C IIC, while fixing the 10-bit addressing mode errata.

8 IIC Control Register 2 (IICC2)

This 10-bit addressing mode is enabled via the IICC2 register.

The IICC2 register controls the general call address function and the 10-bit address extension.

9 10-Bit Address Extension

Setting bit ADEXT allows the IIC to operate using an extended slave address of ten bits. The additional three address bits (AD10:8) are contained within IICC2.

When conducting data transfers using 7-bit addressing, a single address byte is used to identify the slave and indicate the data direction. Therefore, the format was always a calling address byte followed by data bytes for both master transmitter and master receiver communications.

When the 10-bit extended address is enabled, the protocol for initiating data transfers via the IIC is slightly changed.

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
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| 7:6   | General Call Address Enable – The GCAEN bit enables or disables general call address.  
0 General call address is disabled.  
1 General call address is enabled. |
| 5:4   | Address extension – The ADEXT bit controls the number of bits used for the slave address.  
0 7-bit address scheme.  
1 10-bit address scheme. |
| 2:0   | Slave Address – The AD[10:8] field contains the upper three bits of the slave address in the 10-bit address scheme. This field is only valid when the ADEXT bit is set. |

![Figure 1. IIC Control Register (IICC2)](image)

Table 1. IICC2 Field Descriptions

Reset

= Unimplemented or Reserved
In the case of a master transmitter data transfer of two address bytes are required to address the slave. The first address byte always has 0x11110 as its first 5 bits, followed by address bits AD10 and AD9 then the data direction bit. The second address byte consists of the remaining address bits (AD8:1). Once both address bytes have been successfully acknowledged then the master can begin to transmit data to the slave.

For a master receiver data transfer the protocol is more complicated. In this case three address bytes are necessary to address the slave. The first two address bytes are configured exactly as the master transmit data transfer. After these two bytes have been successfully acknowledged, a repeated start signal is sent and the first address byte is resent, but this time with the data direction bit configured to indicate that the slave must transmit data to the master receiver.

A summary of the 10-bit extended address protocol is shown below for both a master transmitter and master receiver data transfers.

A1Slave Address 1st 7 bits 11110 + AD10 + AD9
A2Slave Address 2nd byte AD[8:1]
S = START signal
Ax = Acknowledge bit
Sr = repeated START signal
P = STOP signal

For more information on the IIC, please refer to Freescale document MC9S08AC60 Data Sheet.

## 10 EEPROM Blank Check

With the M74K mask sets, a blank check will display the correct contents of the EEPROM. Other than eliminating the errata behavior, there are no functional differences between 3M05C and M74K. No code considerations are necessary.

## 11 PTA7/ADP7

With the M74K mask sets, the customer is now able to use the port pin as an analog input. However, the pin can no longer be used to wake the part from stop.

If this pin was used to wake the part up from stop, then code must be modified.
12 Controller Area Network (MSCAN)

The MSCAN module on the M74K mask set received improvements to pass CAN conformance testing. Other than eliminating the errata behavior, there are no functional differences between 3M05C and M74K. No code considerations are necessary.

13 Conclusion

Freescale’s M74K mask set of the 9S08DZ60 offers customers a robust solution, addressing the errata found on the 3M05C for automotive and industrial applications. The changes found in the latest mask set do not present any difficulties for programmers or designers familiar with previous versions that wish to migrate to the new version.

All of the new features and enhancements above must be taken into account when migrating from the 3M05C to the M74K.

Finally the user is advised to read the relevant chapters of the latest 9S08DZ60 specifications to ensure that all of the new features and any differences have been fully captured.
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