This application note describes how to use LPC24xx External Memory Controller (EMC) peripheral to drive external SDRAM.
# Revision history

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>20081201</td>
<td>Initial version</td>
</tr>
</tbody>
</table>

---

## Contact information

For additional information, please visit: [http://www.nxp.com](http://www.nxp.com)

For sales office addresses, please send an email to: salesaddresses@nxp.com
1. Introduction

The LPC2400 External Memory Controller (EMC) is an ARM PrimeCell™ MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM and Flash, as well as dynamic memories such as Single Data Rate SDRAM. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

Following is a block diagram of the EMC.

![EMC block diagram](image)

To control a SDRAM memory, the EMC provides the following possible features:
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control CKE and CLKOUT to SDRAM.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2 kbit, 4 kbit, and 8 kbit row address synchronous memory parts.

Eight independently-configurable memory chip selects are supported:
- Pins CSn3 to CSn0 are used to select static memory devices.
- Pins DYCSn3 to DYCSn0 are used to select dynamic memory devices.

The following table shows the address ranges of the chip selects.
The memory controller comprises a static memory controller and a dynamic memory controller. For the EMC register definition, please refer to Table 5–58 of LPC24xx user manual.

2. Hardware connection

Table 2 gives the correspondence between the SDRAM memory pins and the EMC pins and also shows the GPIO configuration for each EMC pin.

In the case of an 8-bit SDRAM memory, the data bus is 8-bit wide and D8-D15 should not be connected to the EMC.

Table 2. SDRAM(K4S561632H) signal to EMC pin correspondence

<table>
<thead>
<tr>
<th>Memory signals</th>
<th>EMC signals</th>
<th>Pin / Port assignment</th>
<th>Signal description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK</td>
<td>CLKOUT0</td>
<td>P2[18]</td>
<td>SDRAM System Clock</td>
</tr>
<tr>
<td>SCKE</td>
<td>CKEOUT0</td>
<td>P2[24]</td>
<td>Clock Enable</td>
</tr>
<tr>
<td>A0 ~ A12</td>
<td>A0 ~ A12</td>
<td>P4[0] ~ P4[12]</td>
<td>Address</td>
</tr>
<tr>
<td>DQ0 ~ DQ15</td>
<td>D0 ~ D15</td>
<td>P3[0] ~ P3[15]</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>nSCS</td>
<td>nDYCS0</td>
<td>P2[20]</td>
<td>Chip Select</td>
</tr>
<tr>
<td>nRAS</td>
<td>nRAS</td>
<td>P2[17]</td>
<td>Row Address Strobe</td>
</tr>
<tr>
<td>nCAS</td>
<td>nCAS</td>
<td>P2[16]</td>
<td>Column Address Strobe</td>
</tr>
<tr>
<td>nWE</td>
<td>nWE</td>
<td>P4[25]</td>
<td>Write Enable</td>
</tr>
<tr>
<td>L(U)DQM</td>
<td>DQMOUT0/1</td>
<td>P2[28]/ P2[29]</td>
<td>Data Input/Output Mask</td>
</tr>
</tbody>
</table>

Figure 2 shows a typical connection between an LPC24xx microcontroller and the Samsung K4S561632H SDRAM memory.
3. SDRAM operation and timing

3.1 SDRAM introduction

SDRAM stands for **Synchronous Dynamic Random Access Memory**. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. A wide range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

The following is SDRAM functional block diagram.
3.2 Commands

The following Truth Table provides a quick reference of several available commands. This is followed by a written description of each command. For each command the LPC24xx SDRAM controller will generate required logic signaling for the connected SDARAM.

<table>
<thead>
<tr>
<th>Name (Function)</th>
<th>CS#</th>
<th>RAS#</th>
<th>CAS#</th>
<th>WE#</th>
<th>DQM</th>
<th>ADDR</th>
<th>DQs</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMMAND INHIBIT (NOP)</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>NO OPERATION (NOP)</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>ACTIVE (Select bank and activate row)</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>Bank/row</td>
<td>X</td>
</tr>
<tr>
<td>READ (Select bank and column, and start READ burst)</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L/H8</td>
<td>Bank/col</td>
<td>X</td>
</tr>
<tr>
<td>WRITE (Select bank and column, and start WRITE burst)</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L/H8</td>
<td>Bank/col</td>
<td>Valid</td>
</tr>
<tr>
<td>BURST TERMINATE</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Active</td>
</tr>
<tr>
<td>PRECHARGE (Deactivate row in bank or banks)</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>Code</td>
<td>X</td>
</tr>
<tr>
<td>AUTO REFRESH or SELF REFRESH (Enter self refresh mode)</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>LOAD MODE REGISTER</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>Op-code</td>
<td>X</td>
</tr>
</tbody>
</table>
3.3 Mode Register

The mode register is used to define the specific operation mode of the SDRAM. This definition includes the selection of burst length, burst type, CAS latency, operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power. At SDRAM initialization, mode register should be set.

The following simple figure describes the mode register.

![Mode Register Description](image)

CAS Latency, CL, is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.
3.4 SDRAM initialization

The SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The recommended power-up sequence for SDRAM is as follows:

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   - Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command to define DS or PASR operating type of the device after normal MRS.

More detail about initialization process will be described in the demo introduction.

3.5 SDRAM timing

In the case where an external SDRAM memory is used, the user has to compute and set the following parameters depending on the information in the memory datasheet.
Table 4. Timing parameters

<table>
<thead>
<tr>
<th>Description</th>
<th>K4S561632(75)</th>
<th>Demo setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>CL/ CLK</td>
<td>CAS latency/SDRAM system clock</td>
<td>2(CLK max100MHz) or 3(CLK max133MHz)</td>
</tr>
<tr>
<td>tRP</td>
<td>precharge command period</td>
<td>20ns(min)</td>
</tr>
<tr>
<td>tRAS</td>
<td>active to precharge command period</td>
<td>45ns(min),100us(max)</td>
</tr>
<tr>
<td>tSREX</td>
<td>self-refresh exit time</td>
<td>____</td>
</tr>
<tr>
<td>tAPR</td>
<td>last-data-out to active command time</td>
<td>____</td>
</tr>
<tr>
<td>tDAL</td>
<td>data-in to active command time</td>
<td>2 CLK + tRP</td>
</tr>
<tr>
<td>tWR</td>
<td>write recovery time</td>
<td>____</td>
</tr>
<tr>
<td>tRC</td>
<td>write recovery time</td>
<td>65ns(min)</td>
</tr>
<tr>
<td>tRFC</td>
<td>auto-refresh period</td>
<td>____</td>
</tr>
<tr>
<td>tXSR</td>
<td>exit self-refresh to active command time</td>
<td>____</td>
</tr>
<tr>
<td>tRRD</td>
<td>active bank A to active bank B latency</td>
<td>15ns(min)</td>
</tr>
<tr>
<td>tMRD</td>
<td>load mode register to active command time</td>
<td>____</td>
</tr>
<tr>
<td>SDRAM_REFRESH</td>
<td>Refresh period</td>
<td>64ms(max)/8192</td>
</tr>
</tbody>
</table>

These parameters give the EMC the flexibility to access a wide variety of external SDRAM.

4. SDRAM Demo

4.1 Hardware environment

IAR_LPC2468 is the test board for this AN. The code can be downloaded to on chip flash via ISP using Flash Magic software or via JTAG using ULink/JLink.

4.2 Software environment

Kei MDK 3.22a is the IDE and toolchain for the software.

4.3 Demo introduction

With the demo, we try to show how to use LPC24xx External Memory Controller (EMC) peripheral to drive external SDRAM. In this demo, LPC24xx will use EMC peripheral to drive one external SDRAM(K4S561632H).
For driving the SDRAM, the EMC_init() function is defined to initialize EMC peripheral which includes port configuration and SDRAM_Test() function is defined for user to write and read SDRAM for test SDRAM.

### 4.4 EMC initialize steps with external SDRAM

Using EMC_init() to initialize EMC.

**Step 1:** configure EMC Pin function and Pin mode.

```c
PINSEL5&=0xF0FCFCC0;  
PINSEL5|=0x05010115;  
PINMODE5&=0xF0FCFCC0;  
PINMODE5|=0x0A02022A;  
//p2.29(DQMOUT1),28(DQMOUT0),24(CKEOUT0),20(DYCS0),18(CLKOUT0)  
//17(RAS),16(CAS)  
// mode=10 (Pin has neither pull-up nor pull-down resistor enabled.)
```

```c
PINSEL6 = 0x55555555;  
PINMODE6 = 0xAAAAAAAA;  
//p3.0-15=D0-15,mode=10
```

```c
PINSEL8 &= 0xC0000000;  
PINSEL8 |= 0x15555555;  
PINMODE8&= 0xC0000000;  
PINMODE8|= 0x2AAAAAAA;  //p4.0-4.14=A0-14,mode=10
```

**Step 2:** enable EMC and set EMC parameters.

```c
PCONP|=0x800;  //enable EMC power  
EMC_CTRL=1;  // enable EMC
```

```c
EMC_DYN_RD_CFG=1;//Configures the dynamic memory read strategy(Command delayed strategy)  
EMC_DYN_RASCAS0|=0x200;EMC_DYN_RASCAS0&=0xFFFFFFFEFF;//CAS latency=2  
EMC_DYN_RASCAS0|=0x3; // RAS latency(active to read/write delay)=3  
EMC_DYN_RP= P2C(SDRAM_TRP);  
EMC_DYN_RAS = P2C(SDRAM_TRAS);  
EMC_DYN_SREX = SDRAM_TXSR;  
EMC_DYN_APR = SDRAM_TAPR;  
EMC_DYN_DAL =SDRAM_TDAL ;  
EMC_DYN_WR = SDRAM_TWR;
```
EMC_DYN_RC = P2C(SDRAM_TRC);
EMC_DYNRFC = P2C(SDRAM_TRFC);
EMC_DYN_XSR = SDRAM_TXSR;
EMC_DYN_RRD = P2C(SDRAM_TRRD);
EMC_DYN_MRD = SDRAM_TMRD;
EMC_DYN_CFG0 = 0x0000680;

// 16 bit external bus, 256 MB (16Mx16), 4 banks, row length = 13, column length = 9

NOTE: Before all EMC timing parameters are configured, their unit should be in ‘CCLK’. The P2C macro is defined to transfer timing parameters from ‘ns’ to ‘CCLK’. If SYS_FREQ == (48)
#define EMC_PERIOD 20.8 // 48MHz
#endif
#define P2C(Period) (((Period<EMC_PERIOD)?0:(unsigned int)((float)Period/EMC_PERIOD))+1)

Step 3: perform SDRAM initialization.

EMC_DYN_CTRL = 0x0183; // NOP
//Issue SDRAM NOP (no operation) command ; CLKOUT runs continuously; All clock enabes are driven HIGH continuously

for(i = 200*30; i;i--);
EMC_DYN_CTRL|=0x100; EMC_DYN_CTRL&=0xFFFFFF7F;
// Issue SDRAM PALL (precharge all) command.
EMC_DYN_RFSH = 1; //Indicates 1X16 CCLKs between SDRAM refresh cycles.
for(i= 128; i; --i); // > 128 clk
EMC_DYN_RFSH = P2C(SDRAM_REFRESH) >> 4;
// Indicates SDRAM_REFRESH time between SDRAM refresh cycles.

EMC_DYN_CTRL|=0x80; EMC_DYN_CTRL&=0xFFFFFEFF;
//Issue SDRAM MODE command.
wtemp = *((volatile unsigned short *)(SDRAM_CS0_BASE | 0x00023000));
/* 8 burst, 2 CAS latency */

EMC_DYN_CTRL = 0x0000; //Issue SDRAM norm command ;
//CLKOUT stop; All clock enabes low

EMC_DYN_CFG0|=0x80000; //Buffer enabled for accesses to DCS0 chip
4.5 SDRAM test

Using the SDRAM_Test() function to write SDRAM and read back from SDRAM. If the data read from the SDRAM is the same as the data written to SDRAM, the function will return 'TRUE', else it will return 'FALSE':

```c
unsigned int SDRAM_Test (void)
{
    unsigned int i;
    // 32 bits access
    for (i = 0; i < 0x2000000; i+=sizeof(unsigned int))
    {
        *(unsigned int *)((unsigned int )&SDRAM_BASE_ADDR+i) = i;
    }
    for (i = 0; i < 0x2000000; i+=sizeof(unsigned int ))
    {
        if (*(unsigned int *)((unsigned int )&SDRAM_BASE_ADDR+i) != i)
        {
            return(FALSE);
        }
    }
    // 16 bits access
    for (i = 0; i < 0x10000; i+=sizeof(unsigned short))
    {
        *(unsigned short*)((unsigned int)&SDRAM_BASE_ADDR+i) = i;
    }
    for (i = 0; i < 0x10000; i+=sizeof(unsigned short))
    {
        if (*(unsigned short*)((unsigned int)&SDRAM_BASE_ADDR+i) != i)
        {
            return(FALSE);
        }
    }
    // 8 bits access
    for (i = 0; i < 0x100; i+=sizeof(unsigned char))
    {
        *(unsigned char*)((unsigned int)&SDRAM_BASE_ADDR+i) = i;
    }
```
for (i = 0; i < 0x100; i += sizeof(unsigned char))
{
    if (*((unsigned char*)((unsigned int)&SDRAM_BASE_ADDR+i) != i)
    {
        return(FALSE);
    }
}
return(TRUE);

5. Reference

[2] K4S56xx32h datasheet, Rev 1.0, Samsung electronics
6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is for the customer’s own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.
7. Contents

1. Introduction ......................................................... 3
2. Hardware connection ........................................ 4
3. SDRAM operation and timing ...................................... 5
  3.1 SDRAM introduction ........................................... 5
  3.2 Commands ......................................................... 6
  3.3 Mode Register .................................................... 7
  3.4 SDRAM initialization ........................................... 8
  3.5 SDRAM timing .................................................... 8
4. SDRAM Demo ...................................................... 9
  4.1 Hardware environment ....................................... 9
  4.2 Software environment ....................................... 9
  4.3 Demo introduction ............................................ 9
  4.4 EMC initialize steps with external SDRAM ............ 10
  4.5 SDRAM test ..................................................... 12
5. Reference ........................................................... 13
6. Legal information .............................................. 14
  6.1 Definitions ........................................................ 14
  6.2 Disclaimers ....................................................... 14
  6.3 Trademarks ...................................................... 14
7. Contents ............................................................. 15