Clocking Options for Stellaris® Family
Microcontrollers

Application Note

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Introduction

This application note discusses the clocking options available on the Stellaris family microcontrollers, including use and configuration of the Phase Locked Loop (PLL).

Stellaris Clock Tree

The two clock sources for the Stellaris microcontrollers are the main oscillator and the internal oscillator. Both sources have the ability to drive the system clock, however, the device cannot boot from the internal oscillator. With the oscillator source selected (see Figure 1), the remainder of the system clocking tree is configured by choosing the appropriate clock dividers (SYSDIV and PWMDIV).

Figure 1. Clock Tree

Application software chooses whether to use the PLL based on the value of the BYPASS signal. When the PLL is in use, it always outputs a 200-MHz clock signal, and when combined with the system divider (SYSDIV), generates the system clock.

The clock that is fed into the PWM module is derived from the system clock. In applications requiring a slower PWM clock, the PWM divider (PWMDIV) can be applied to the clock signal before it reaches the PWM module.

The ADC clock uses a constant divider that assumes a 200-MHz source, meaning that for the ADC clock to meet the required operating range of 14–18 MHz, the PLL must be enabled and used.

Oscillator Sources

The main oscillator allows either a crystal or single-ended input clock signal. Cost-sensitive applications typically use an external crystal with the on-chip oscillator circuit since it is the most cost-effective solution. It is also possible to use the internal oscillator to clock the device after the boot process has completed.

Crystal

A crystal is used with the internal oscillator circuit by connecting the crystal to the OSC1 and OSC2 pins of the Stellaris device (along with two capacitors) as shown in Figure 2 on page 5. The values of C1 and C2 are 15 pF for all crystals specified to work with the PLL (3.579545–8.192 MHz).
Single-Ended Clock
The second option for driving the main oscillator is using a single-ended clock source, such as a crystal oscillator, or even a function generator (for debug purposes). Using such a clock source does not require the on-chip oscillator circuit, and therefore does not require the OSC2 pin (see Figure 3 on page 6). The OSC2 pin is left floating in this configuration.

When using a single-ended clock source with the PLL, one of the supported crystal frequencies must be used (see Table 1 on page 6).

Internal Oscillator
It is also possible to use the internal oscillator (or the internal oscillator divided by four) to clock the device once the boot process has completed. The oscillator source is changed by modifying the OSCSRC field of the RCC register in the System Control module.

A major hindrance to using the internal oscillator is that its accuracy is only guaranteed to be within ±50% of its ideal operating frequency of 15 MHz. Having such a large variance between devices practically eliminates the usefulness of the internal oscillator as a clock source in a real-world application. The primary use for the internal oscillator is for performing an internal clock check on the main oscillator source.
Using the PLL

The PLL requires specific input clock frequencies in order to run at the desired 200 MHz. Crystals or single-ended sources ranging in frequency from 3.579545–8.192 MHz are supported. See Table 1 for the full list of supported crystal frequencies.

Table 1. Supported Crystal Frequencies

<table>
<thead>
<tr>
<th>Crystal Frequency (MHz)</th>
<th>PLL Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.579545 MHz</td>
<td>5.12 MHz</td>
</tr>
<tr>
<td>3.6864 MHz</td>
<td>6 MHz (reset value)</td>
</tr>
<tr>
<td>4 MHz</td>
<td>6.144 MHz</td>
</tr>
<tr>
<td>4.096 MHz</td>
<td>7.3728 MHz</td>
</tr>
<tr>
<td>4.9152 MHz</td>
<td>8 MHz</td>
</tr>
<tr>
<td>5 MHz</td>
<td>8.192 MHz</td>
</tr>
</tbody>
</table>

When a crystal or single-ended source with a supported frequency is used, the Stellaris device uses an internal look-up table to populate the PLL parameters in the XTAL to PLL Translation (PLLCFG) register. Using unsupported frequencies with the PLL can create faulty operation of the ADC module (if present).
Example 1. Configuring the PLL with the Driver Library
This example shows how to configure the PLL using the StellarisWare® Peripheral Driver Library functions. The Driver Library is a software bundle of example drivers provided free by Texas Instruments. To download the software, visit the www.luminarymicro.com website.

Configuring the PLL with the Driver Library is simple; it only requires a call to the `SysCtlClockSet` function. To configure the PLL to use a 6-MHz crystal and to run at a 20-MHz system clock, the function call is as shown in Code Segment 1.a.

**Code Segment 1.a. Configure PLL with `SysCtlClockSet`**
```c
SysCtlClockSet(SYSCTL_SYSDIV_10 | SYSCTL_USE_PLL | SYSCTL_OSC_MAIN | SYSCTL_XTAL_6MHZ);
```

The configuration parameters passed to the function are modifiable to fit the needs of the application. Typically, the only parameter that might change is the system divider since the oscillator frequency is usually fixed. The PLL is bypassed by changing the `SYSCTL_USE_PLL` parameter to `SYSCTL_USE_OSC`.

Example 2. Configuring the PLL with Direct Register Writes
When the Driver Library functions are not used, the PLL is configured using direct register writes to the **Run-Mode Clock Configuration (RCC)** register. The steps required to successfully change the PLL-based system clock are:

1. Bypass the PLL and system clock divider by setting the **BYPASS** bit and clearing the **USESYS** bit in the **RCC** register. This configures the system to run off a “raw” clock source (using the main oscillator or internal oscillator) and allows for the new PLL configuration to be validated before switching the system clock to the PLL.

2. Select the crystal value (**XTAL**) and oscillator source (**OSCSRC**), and clear the **PWRDN** and **OE** bits in **RCC**. Setting the **XTAL** field automatically pulls valid PLL configuration data for the appropriate crystal, and clearing the **PWRDN** and **OE** bits powers and enables the PLL and its output.

3. Select the desired system divider (**SYSDIV**) and set the **USESYS** bit in **RCC**. The **SYSDIV** field determines the system frequency for the microcontroller.

4. Wait for the PLL to lock by polling the **PLLLRIS** bit in the **Raw Interrupt Status (RIS)** register. If the PLL doesn’t lock, the configuration is invalid.

5. Enable use of the PLL by clearing the **BYPASS** bit in **RCC**.

**Important:** If the **BYPASS** bit is cleared before the PLL locks, it is possible to render the device unusable.

**Conclusion**
Stellaris microcontrollers must use an external oscillator source to boot, but can be configured to use the internal oscillator to clock the device if needed. For most applications, an inexpensive crystal is all that is required to clock the device, and the wide range of supported crystal frequencies allows flexibility in choosing an oscillator to use with the PLL.
References

The following documents are available for download at www.luminarymicro.com:

- Stellaris microcontroller data sheet, Publication Number DS-LM3Snnn (where nnn is the part number for that specific Stellaris family device)
- StellarisWare® Driver Library
- StellarisWare® Driver Library User’s Manual, publication number SW-DRL-UG
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