Powering OMAP™3 With TPS65023: Design-In Guide

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ABSTRACT
This document details the design considerations of a power management unit solution for the OMAP™3 processor using the TPS65023 device.

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1 Introduction

The OMAP35x Applications Processors have a diverse set of power management features which potentially enable lower cost power solutions based on your application. This design-in guide describes a power solution based on the TPS65023 device. This guide can be used to evaluate this solution for your design, or help you make decisions when designing in this solution.

2 Power Requirements and Features of OMAP35x

A TPS65023-based power solution can power any device in the OMAP35x family (OMAP3503, OMAP3515, OMAP3525, and OMAP3530). The following section describes the specifications and power management features of these devices.

2.1 Power Specifications

The following tables detail the power requirements for each OMAP35x device that is supported by a TPS65023-based power solution. Note that the only difference in power lies in the amount of current required by the VDD_CORE and VDD_MPU_IVA voltage rails. Otherwise, the specifications are identical.

### Table 1. OMAP3503 Power Specifications

<table>
<thead>
<tr>
<th>POWER RAIL</th>
<th>VOLTAGE</th>
<th>TOLERANCE</th>
<th>Imax (mA)</th>
<th>SEQUENCING ORDER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core VDD_MPU</td>
<td>0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)</td>
<td>±5%</td>
<td>680</td>
<td>4</td>
</tr>
<tr>
<td>Core VDD_CORE</td>
<td>0.95 V, 1 V, 1.15 V (1)</td>
<td>±5%</td>
<td>320</td>
<td>3</td>
</tr>
<tr>
<td>I/O VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM</td>
<td>1.8 V</td>
<td>±5%</td>
<td>147</td>
<td>1</td>
</tr>
<tr>
<td>I/O VDDS_DPLL_PER, VDDS_DPLL_DLL</td>
<td>1.8 V</td>
<td>±5%</td>
<td>40</td>
<td>2</td>
</tr>
<tr>
<td>I/O VDDA_DAC</td>
<td>1.8 V</td>
<td>±5%</td>
<td>65</td>
<td>After reset</td>
</tr>
<tr>
<td>I/O VDDS_MMC1, VDDS_MMC1A</td>
<td>1.8 V</td>
<td>±5%</td>
<td>22</td>
<td>After reset (see MMC Boot for more information)</td>
</tr>
<tr>
<td>I/O VDDS_MMC1A</td>
<td>3 V</td>
<td>±10%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The preceding power numbers assume that SmartReflex™ AVS is implemented at 90°C.

(1) See the latest OMAP35x Operating Condition Addendum for the most current voltage values.

### Table 2. OMAP3515 Power Specifications

<table>
<thead>
<tr>
<th>POWER RAIL</th>
<th>VOLTAGE</th>
<th>TOLERANCE</th>
<th>Imax (mA)</th>
<th>SEQUENCING ORDER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core VDD_MPU</td>
<td>0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)</td>
<td>±5%</td>
<td>680</td>
<td>4</td>
</tr>
<tr>
<td>Core VDD_CORE</td>
<td>0.95 V, 1 V, 1.15 V (1)</td>
<td>±5%</td>
<td>433</td>
<td>3</td>
</tr>
<tr>
<td>I/O VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM</td>
<td>1.8 V</td>
<td>±5%</td>
<td>147</td>
<td>1</td>
</tr>
<tr>
<td>I/O VDDS_DPLL_PER, VDDS_DPLL_DLL</td>
<td>1.8 V</td>
<td>±5%</td>
<td>40</td>
<td>2</td>
</tr>
<tr>
<td>I/O VDDA_DAC</td>
<td>1.8 V</td>
<td>±5%</td>
<td>65</td>
<td>After reset</td>
</tr>
<tr>
<td>I/O VDDS_MMC1, VDDS_MMC1A</td>
<td>1.8 V</td>
<td>±5%</td>
<td>22</td>
<td>After reset (see MMC Boot for more information)</td>
</tr>
<tr>
<td>I/O VDDS_MMC1A</td>
<td>3 V</td>
<td>±10%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The preceding power numbers assume that SmartReflex™ AVS is implemented at 90°C.

(1) See the latest OMAP35x Operating Condition Addendum for the most current voltage values.

OMAP, that SmartReflex, SmartReflex are trademarks of Texas Instruments.

I²C is a trademark of Philips Corporation.
Table 3. OMAP3525 Power Specifications

<table>
<thead>
<tr>
<th>POWER RAIL</th>
<th>VOLTAGE</th>
<th>TOLERANCE</th>
<th>Imax (mA)</th>
<th>SEQUENCING ORDER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core VDD_MPU_IVA</td>
<td>0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)</td>
<td>±5%</td>
<td>1140</td>
<td>4</td>
</tr>
<tr>
<td>Core VDD_CORE</td>
<td>0.95 V, 1 V, 1.15 V (1)</td>
<td>±5%</td>
<td>330</td>
<td>3</td>
</tr>
<tr>
<td>I/O VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM</td>
<td>1.8 V</td>
<td>±5%</td>
<td>147</td>
<td>1</td>
</tr>
<tr>
<td>I/O VDDS_DPLL_PER, VDDS_DPLL_DLL</td>
<td>1.8 V</td>
<td>±5%</td>
<td>40</td>
<td>2</td>
</tr>
<tr>
<td>I/O VDDA_DAC</td>
<td>1.8 V</td>
<td>±5%</td>
<td>65</td>
<td>After reset</td>
</tr>
<tr>
<td>I/O VDDS_MMC1, VDDS_MMC1A</td>
<td>1.8 V</td>
<td>±5%</td>
<td>22</td>
<td>After reset (see MMC Boot for more information)</td>
</tr>
</tbody>
</table>

The preceding power numbers assume that SmartReflex™ AVS is implemented at 90°C.

(1) See the latest OMAP35x Operating Condition Addendum for the most current voltage values.

Table 4. OMAP3530 Power Specifications

<table>
<thead>
<tr>
<th>POWER RAIL</th>
<th>VOLTAGE</th>
<th>TOLERANCE</th>
<th>Imax (mA)</th>
<th>SEQUENCING ORDER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core VDD_MPU_IVA</td>
<td>0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)</td>
<td>±5%</td>
<td>1140</td>
<td>4</td>
</tr>
<tr>
<td>Core VDD_CORE</td>
<td>0.95 V, 1 V, 1.15 V (1)</td>
<td>±5%</td>
<td>433</td>
<td>3</td>
</tr>
<tr>
<td>I/O VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM</td>
<td>1.8 V</td>
<td>±5%</td>
<td>147</td>
<td>1</td>
</tr>
<tr>
<td>I/O VDDS_DPLL_PER, VDDS_DPLL_DLL</td>
<td>1.8 V</td>
<td>±5%</td>
<td>40</td>
<td>2</td>
</tr>
<tr>
<td>I/O VDDA_DAC</td>
<td>1.8 V</td>
<td>±5%</td>
<td>65</td>
<td>After reset</td>
</tr>
<tr>
<td>I/O VDDS_MMC1, VDDS_MMC1A</td>
<td>1.8 V</td>
<td>±5%</td>
<td>22</td>
<td>After reset (see MMC Boot for more information)</td>
</tr>
</tbody>
</table>

The preceding power numbers assume that SmartReflex™ AVS is implemented at 90°C.

(1) See the latest OMAP35x Operating Condition Addendum for the most current voltage values.

2.2 Power-Up Sequencing

Figure 1 shows the power-up sequencing requirements of OMAP35x. The description of the power-up sequence follows.

1. VDDS_WKUP_BG, VDDS_MEM, VDDS, and VDDS_SRAM are all 1.8-V rails and are tied to the same power supply. These are ramped first, ensuring a valid level on the I/O domain. In the example block diagram (1), these rails are powered by the DCDC3 in the TPS65023.
2. During the entire power-up sequence, the power-on-reset signal SYS_NRESPWRON must be held low until all rails and clocks are stable. This is accomplished using the RESPWRON output of the TPS65023 and the appropriate capacitor connected to T_RESPWRON to achieve the desired delay time. See SYS_nRESPWRON Timing for more information.
3. Both the 32-kHz and the high-frequency clock need to start oscillating and be stable.
4. After 1.8 V is stabilized, VDD_CORE can start ramping.
5. After VDD_CORE is stabilized, VDD_MPU_IVA can start ramping.
6. After 1.8 V is stabilized, VDDS_DPLL_DLL and VDDS_DPLL_PER (rails are tied to the same power supply) can ramp during or after VDD_CORE and VDD_MPU_IVA ramp.
7. Once all of the preceding power rails have stabilized, and 32-kHz and the high-frequency clock have stabilized, then SYS_NRESPWRON can be released.
8. Other power supplies, such as VDDS_MMC1, VDDS_MMC1A, VDDS_DAC, etc., can be turned on or off depending on the application.
2.3 **Power-Down Sequencing**

When using the TPS65023 power solution, power down is achieved by removing the input voltage VBAT. When this occurs, all voltages ramp down at the same time, and the ramp rate of each voltage is generally determined by the load on that voltage.

During power down, all signals driving OMAP™3 must have a voltage level equal or less than the I/O voltage of OMAP™3 to avoid driving pins that are unpowered. For example, the schematic example of Figure 2 shows the 32-kHz clock gated by a 1.8-V Power Good signal. This ensures that this clock circuit does not drive the OMAP™3 input clock pins when the 1.8 V is removed from OMAP™3.
2.4 OMAP35x Power Management Features

The OMAP35x Application Processors have a rich set of features that make aggressive power optimizations feasible in a user application. These features include DVFS (dynamic voltage frequency scaling) and SmartReflex™ AVS (adaptive voltage scaling). Both of these features allow for the lowest power operation depending on the OMAP35x processing requirements. In short, DVFS allows the user to change between the OMAP35x’s operating points (voltages) depending on the device’s operating frequency. Depending on your application, you may want to be able to move among these voltage levels during operation to reduce power consumption. SmartReflex™ AVS optimizes each of these operating points based on wafer process differences, temperature, and silicon degradation.

2.4.1 Dynamic Voltage and Frequency Scaling

DVFS is a power management technique used while active processing is going on in the system-on-chip (SoC). This technique matches the operating frequency of the hardware to the performance requirement of the active application scenario. Whenever clock frequencies are lowered, operating voltages can be lowered as well to achieve power savings. OMAP35x supports this technique on VDD_MPU_IVA and VDD_CORE power rails by defining discrete voltage values for these power rails and the accompanying maximum clock frequencies allowed for the modules supplied by those power rails. Each operating voltage and accompanying maximum clock frequency specification is called an operating performance point (OPP). The following tables show the OPP definitions for VDD_MPU_IVA and VDD_CORE.

Table 5. VDD_MPU_IVA Operating Points

<table>
<thead>
<tr>
<th>PROCESSOR OPP</th>
<th>VDD_MPU_IVA</th>
<th>ARM Max MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>1.35</td>
<td>600</td>
</tr>
<tr>
<td>4</td>
<td>1.27</td>
<td>550</td>
</tr>
<tr>
<td>3</td>
<td>1.20</td>
<td>500</td>
</tr>
<tr>
<td>2</td>
<td>1.00</td>
<td>250</td>
</tr>
<tr>
<td>1</td>
<td>0.95</td>
<td>125</td>
</tr>
</tbody>
</table>
### Powering Requirements

**Table 6. VDD_CORE Operating Points**

<table>
<thead>
<tr>
<th>INTERCONNECT/PERIPHERALS OPP</th>
<th>VDD_CORE</th>
<th>L3 Max MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>1.15</td>
<td>166</td>
</tr>
<tr>
<td>2</td>
<td>1.00</td>
<td>100</td>
</tr>
<tr>
<td>1</td>
<td>0.95</td>
<td>41.5</td>
</tr>
</tbody>
</table>

See the latest OMAP™3 Operating Condition Addendum for the most current voltage values.

A TPS65023 power solution supports DVFS for OMAP35x by meeting the requirements shown in **Table 7**.

**Table 7. TPS65023 Power Solution Support for DVFS**

<table>
<thead>
<tr>
<th>Power IC Requirement for DVFS</th>
<th>Does TPS65023 based power solution implement the requirement?</th>
<th>How TPS65023 power module for the OMAP3EVM enables DVFS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Support all five DVFS voltage values (0.95 V, 1 V, 1.2 V, 1.27 V, and 1.35 V) defined for VDD_MPU</td>
<td>Yes. TPS65023 DCDC1 supports full voltage range and can adjust in 25-mV increments</td>
<td>TPS65023 DCDC1 used to power VDD_MPU_IVA rail</td>
</tr>
<tr>
<td>Support all three DVFS voltage values (0.95 V, 1 V, and 1.15 V) defined for VDD_CORE</td>
<td>No. TPS65023 only supports a fixed voltage on DCDC2 for VDD_CORE.</td>
<td>TPS65023 DCDC2 fixed to 1.15 V used to power VDD_CORE rail</td>
</tr>
<tr>
<td>I2C™ interface for setting output voltage to any of the values defined for DVFS</td>
<td>Yes. TPS65023 supports full speed I2C bus available for controlling voltage output for DCDC1 only.</td>
<td>I2C bus of TPS65023 connected to OMAP35x I2C bus</td>
</tr>
</tbody>
</table>

### 2.4.2 SmartReflex™ Adaptive Voltage Scaling

AVS is a power management technique that can be used to refine system power consumption at a given OPP. The DVFS technique defines safe voltages for the OPPs so that all manufactured devices can meet the maximum frequency specifications for the OPPs. However, the silicon manufacturing process yields a distribution of devices, some (called strong or hot devices) of which can meet the frequency specifications at lower operating voltages than the conservative values defined by DVFS. SmartReflex™ AVS has been implemented by Texas Instruments to continuously adapt the operating voltage to the process properties of individual devices in order to maximize power savings for active scenarios. The OMAP35x integrates specialized hardware to enable SmartReflex™ AVS on VDD_MPU_IVA and VDD_CORE. This special hardware can be used to implement Class-3 or Class-2 SmartReflex™.

- **Class-2 SmartReflex™**: The special hardware monitors real-time performance; small software loop runs on ARM processor to change voltage whenever necessary.
- **Class-3 SmartReflex™**: The special hardware has a dedicated hardware loop to dynamically monitor performance and adjust voltage without ARM processor intervention.

Equivalent power savings can be achieved with either implementation.

A TPS65023 power solution supports SmartReflex™ for OMAP35x by meeting the requirements shown in **Table 8**. See Enabling Class 2 SmartReflex for more implementation details.

**Table 8. TPS65023 Power Solution for SmartReflex™ Implementation**

<table>
<thead>
<tr>
<th>Power IC Requirement for SmartReflex™ Implementation</th>
<th>Does TPS65023-based power solution implement the requirement?</th>
<th>How TPS65023 power module for the OMAP3EVM enables SmartReflex™ Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-speed (or full-speed) I2C bus for setting output voltage</td>
<td>Yes. FS I2C bus available.</td>
<td>I2C connections present between TPS65023 and OMAP35x I2C bus</td>
</tr>
<tr>
<td>Voltage programmability in steps over the range 0.8 V to 1.35 V</td>
<td>Yes only for VDD_MPU_IVA. Can scale the output voltage between 0.8 V to 1.6 V with voltage steps down to 25 mV.</td>
<td>Makes use of this property of TPS65023 used to power VDD_MPU_IVA</td>
</tr>
<tr>
<td>(For Class-3 SmartReflex™) Ability to effect voltage change with a single I2C register write</td>
<td>No. TPS65023 requires two I2C writes to change voltage and cannot support Class 3 SmartReflex™</td>
<td>No support</td>
</tr>
</tbody>
</table>
2.4.3 Static/Standby Leakage Management

Static/standby leakage management (SLM) is the combination of techniques used to achieve lowest power consumption during system idle time, when a system-on-chip (SoC) performs no useful processing. The OMAP35x supports various options for low-power standby states that trade-off level of power savings with speed of wake-up latency. The level of power savings during standby is determined by whether internal memories and logic are retained or powered down, whether clocks are on or off, and whether external voltage regulators are kept on or off.

Several SLM features are built into the OMAP35x architecture to enable low-power standby modes. In addition, OMAP35x supports features for achieving further standby power savings by putting system components external to the OMAP™ SoC into lower power states. Notable among these are control signals for gating external clock and power sources.

- **SYS_CLKREQ** is a signal used to gate the high-frequency clock when it is not needed. The OMAP35x can be set up to automatically deassert the sys_clkreq in full-chip retention and/or off modes.
- **SYS_OFF_MODE** is a signal used to indicate to external voltage regulators when they can be shut down.

OMAP35x supports a standby mode called off-mode, which is the lowest power state from which the device can wake up autonomously. In OMAP35x off-mode, system state is saved in external memory that can be put into self-refresh mode, most of the SoC is off, but a small wakeup domain stays powered on and operational at 32 kHz to monitor for wake-up events. The sys_clkreq is used to sequence an external clock source, while the sys_off_mode signal is used to sequence power during transitions into and out of the off-mode. The ability to shut off most of the external voltage supplies in this off-mode saves additional power dissipation in the voltage regulators. Alternatively using the sys_off_mode pin, OMAP35x supports I2C commands for VDD_MPU_IVA and VDD_CORE sequencing during off-mode transitions.

A TPS65023 power solution supports OMAP35x SLM by meeting the requirements shown in Table 9.

### Table 9. TPS65023 Power Solution Support for SLM

<table>
<thead>
<tr>
<th>Power IC Requirement for SLM</th>
<th>Does TPS65023-based power solution implement the requirement?</th>
<th>How TPS65023 power module for the OMAP3EV3 enables SLM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ability to gate high-frequency clock source with IO signal for standby power savings</td>
<td>Yes. Can be taken care of in hardware with SYS_CLKREQ. See High Frequency Clock Circuit.</td>
<td>Not supported on power module</td>
</tr>
<tr>
<td>(For SLEEP mode) Ability to lower voltage on VDD_MPU_IVA power source to lowest OPP via I2C</td>
<td>Yes. Supports I2C register write to DEFCORE and GO bit to lower voltage to OPP</td>
<td>Use I2C2 write to lower voltage on DCDC1 to OPP1.</td>
</tr>
<tr>
<td>(For SLEEP mode) Ability to lower voltage on VDD_CORE power source to lowest OPP via I2C</td>
<td>No. VDD_CORE voltage cannot be altered</td>
<td>DCDC2 voltage cannot be altered</td>
</tr>
<tr>
<td>(For OFF mode) Ability to turn off/on VDD_MPU_IVA power source with SYS_OFF_MODE signal or a single register write to the power IC over I2C</td>
<td>Yes. Supports I2C register write to REG_CTRL register of TPS65023 to turn off DCDC1 (VDD_MPU_IVA)</td>
<td>Use I2C2 write to disable DCDC1.</td>
</tr>
</tbody>
</table>
Table 9. TPS65023 Power Solution Support for SLM (continued)

<table>
<thead>
<tr>
<th>Power IC Requirement for SLM</th>
<th>Does TPS65023-based power solution implement the requirement?</th>
<th>How TPS65023 power module for the OMAP3EVM enables SLM</th>
</tr>
</thead>
<tbody>
<tr>
<td>(For OFF mode) Ability to turn on/off VDD_CORE power source with SYS_OFF_MODE signal or a single register write to the power IC over I2C</td>
<td>Yes. Supports I2C register write to REG_CTRL register of TPS65023 to turn off DCDC2 (VDD_CORE)</td>
<td>Use I2C2 write to disable DCDC2</td>
</tr>
</tbody>
</table>

3 TPS65023 Design-In Considerations

Figure 3 is a block diagram of one example of a complete power solution using the TPS65023 devices to power OMAP™3. The rest of the section details each design consideration to tailor the power solution to your needs.

Figure 3. TPS65023 Power Solution Block Diagram
3.1 Reset

3.1.1 SYS_nRESPWRON Rise Time

The OMAP35x data sheet states that the maximum rise/fall time for SYS_nRESPWRON is 10 ns (see the following highlighted sections extracted from data sheets).

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>AH25</td>
<td>NA</td>
<td>sys_nrespwr</td>
<td>0</td>
<td>I</td>
<td>Z</td>
<td>I</td>
<td>NA</td>
<td>vdds</td>
<td>Yes</td>
<td>NA</td>
<td>NA</td>
<td>LVCMOS</td>
</tr>
</tbody>
</table>

**PARAMETER** | **MIN** | **NOM** | **MAX** | **UNIT**

**STANDARD LVCMOS**

- $V_{IH}^{(6)}$: High-level input voltage
  
  $0.65 \times vdd^{(5)} - vdds \div 0.3$ V

- $V_{IL}^{(6)}$: Low-level input voltage
  
  $-0.3$ V

- $V_{OH}$: High-level output voltage, driver enabled, pullup or pulldown disabled
  
  $I_O = I_{OH}$ or $I_O = -2$ mA

  $vddsy^{(5)} - 0.45$ V

  $I_O = I_{OH} \leq -2$ mA

  $vddsy^{(5)} - 0.40$ V

- $V_{OL}$: Low-level output voltage with driver enabled, pullup or pulldown disabled
  
  $I_O = I_{OL}$ or $I_O = 2$ mA

  $0.45$ V

  $I_O = I_{OL} \leq 2$ mA

  $0.40$ V

- $t_T$: Input transition time (rise time, $t_R$ or fall time, $t_F$ evaluated between 10% and 90% at PAD)
  
  $0$ ns

  $10^{(2)}$ ns

- $I_I$: Input current with $V_I = V_{Li}$ max
  
  $-1$ μA

  $1$ μA

- $I_{OZ}$: Off-state output current for output in high impedance with driver only, disabled
  
  $-20$ μA

  $20$ μA

In order to meet this requirement, a push-pull output buffer is required, with rise/fall time of <10 ns.

The TPS65023 RESPWRON output is open drain and requires a buffer or gate with a fast rise time to meet the OMAP™3 requirement. If multiple reset sources are needed, you can use an AND gate as shown in Figure 4 to provide fast rise time for all reset sources.

![Figure 4. Circuitry to Combine Multiple Reset Sources](image-url)
3.1.2 SYS_nRESPWRON Timing

Typical 32-kHz oscillators on the market can have up to a 1-second maximum to stabilize. This poses a challenge in the power-up sequencing in that the reset signal must be maintained low throughout this stabilization time in order to properly reset OMAP™3. You can achieve this lengthy reset time using the TRESPWRON input of the TPS65023. Consult the TPS65023 data sheet for detailed information. By connecting a capacitor to ground to this signal, you can adjust the delay time of the reset output RESPWRO.

\[ t_{\text{reset}} = 2 \times 128 \times \left( \frac{1\text{V} - 0.25\text{V} \times C_{\text{reset}}}{2\mu\text{A}} \right) \]

Where:
- \( t_{\text{reset}} \) is the reset delay time
- \( C_{\text{reset}} \) is the capacitor connected to the TRESPWRON pin

For example, to achieve a 1-second reset delay, you can use a 10-nF capacitor to ground. See the TPS65023 data sheet (SLVS670) for more detailed information.

3.2 Clocks

3.2.1 Clock Rise/Fall Time

OMAP™3 clocks (both 32-kHz and high-frequency clocks) also have strict rise/fall requirements. Note the excerpts from the data manual below:

<table>
<thead>
<tr>
<th>PAD</th>
<th>CLOCK FREQUENCY</th>
<th>STABILITY</th>
<th>DUTY CYCLE</th>
<th>JITTER</th>
<th>TRANSITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>sys_32k</td>
<td>32.768 kHz</td>
<td>±200 ppm</td>
<td>—</td>
<td>—</td>
<td>&lt;20 ns</td>
</tr>
<tr>
<td>sys_xtalout</td>
<td>12, 13, 16.8 or 19.2 MHz</td>
<td>Crystal</td>
<td>±25 ppm</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>sys_xtalin</td>
<td>12, 13, 16.8, 19.2, 26 or 38.4 MHz</td>
<td>Square</td>
<td>±50 ppm</td>
<td>45% to 55%</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>sys_alctlk</td>
<td>48, 54, or up to 59 MHz</td>
<td>±50 ppm</td>
<td>40% to 60%</td>
<td>&lt;1%</td>
<td>&lt;10 ns</td>
</tr>
</tbody>
</table>

In order to meet these rise/fall times, a push-pull buffer is required to provide a faster edge on both clocks. See the diagrams in sections 32 kHz Clock Circuit and High Frequency Clock Circuit.

3.2.2 Clock Gating

When using an external oscillator for the high-frequency clock, the OMAP3 SYS_CLKREQ signal is used to request the high-frequency clock. This signal can be used to gate the clock on power up while OMAP™3 is going through its power-up sequence.

![Figure 5. Clock Squarer Source Connection](image-url)
Generally, the 32-kHz oscillator is powered off the 1.8-V supply. Use this as a condition before applying the 32 kHz to the I/Os of OMAP™3.

### 3.2.3 32-kHz Clock Circuit

If the 32-kHz oscillator you choose exceeds the rise/fall time limit, a push-pull output buffer must be used to create a faster edge. Generally, the 32-kHz oscillator is powered off the 1.8-V supply. Use this as a gating condition before applying the 32 kHz to the I/Os of OMAP™3. The TPS65023 provides an adequate 1.8-V power-good signal.

![Push-Pull Buffer Circuitry on 32-kHz Clock](image)

**Figure 6. Push-Pull Buffer Circuitry on 32-kHz Clock**

### 3.2.4 High-Frequency Clock Circuit

OMAP™3 requires a high-frequency clock for normal operation. OMAP™3 accepts two different types of input clock sources:

- A crystal can be used in combination with the internal OMAP™3 oscillator for frequencies 12, 13, 16.8, or 19.2 MHz.
- A square oscillator can be used with the OMAP™3 oscillator in bypass mode for frequencies 12, 13, 16.8, 19.2, 26, or 38.4 MHz

When an external oscillator is used, it has strict rise/fall time restrictions of less than 2.5 ns.

**Table 10. Clock Source Requirements With External Oscillator**

<table>
<thead>
<tr>
<th>PAD</th>
<th>CLOCK FREQUENCY</th>
<th>STABILITY</th>
<th>DUTY CYCLE</th>
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<td>sys_32k</td>
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<tr>
<td>sys_xtalout</td>
<td>12, 13, 16.8 or 19.2 MHz</td>
<td>Crystal</td>
<td>±25 ppm</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>sys_xtalin</td>
<td>12, 13, 16.8, 19.2, 26 or 38.4 MHz</td>
<td>Square</td>
<td>±50 ppm</td>
<td>45% to 55%</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>sys_altclk</td>
<td>48, 54, or up to 59 MHz</td>
<td>±50 ppm</td>
<td>40% to 60%</td>
<td>&lt;1%</td>
<td>&lt;10 ns</td>
</tr>
</tbody>
</table>
In order to meet these requirements, a push-pull buffer is required before the clock input of OMAP™3.

![Figure 7. Push-Pull Buffer Circuitry on 26-MHz Clock](image)

### 3.3 Power Devices

A TPS65023-based power solution integrates many different power sources required to power up OMAP™3 devices.

The TPS65023 features the following benefits to make it an ideal PMIC for OMAP™3:

- Contains three DC-DC converters and two LDOs with enough supply current for all OMAP35x family devices
- Each DC-DC converter and the LDOs can be sequenced using external sense signals and enables.
- The second LDO inside the TPS65023 can be used to power OMAP™3 MMC rail. For power-sensitive applications, it is recommended to power the MMC rail off of a separate LDO to allow you to enable/disable the voltage separate from the PLL.
- Provides adjustable reset circuitry to control reset timing
- Provides adequate default voltages on power up
- Provides I2C control of all power sources
- Provides voltage scaling and adequate voltage granularity to allow implementation of DVFS and SmartReflex™ AVS.

For applications requiring VDAC voltage, a separate LDO (TPS72118) is used which provides the proper 1.8 V, 150-mA maximum current. By connecting an OMAP™3 GPIO, you can enable/disable this power source as the application needs it. An example schematic is below. If you are not using the video DAC on OMAP™3, you do not need to include this LDO in your design.

![Figure 8. LDO Circuitry to Provide VDAC Voltage](image)

Note that while the voltage for VDD_MPU_IVA (connected to DCDC1) can be adjusted via I2C, the voltage for VDD_CORE (DCDC2) has to be fixed. The voltage level is fixed by means of external circuitry (see the TPS65023 documentation for details). To enable full performance, you must fix this voltage at the highest OPP (1.15 V), however, if your application only requires lower performance levels, you can adjust your external circuitry to output a lower fixed voltage.
3.4  **Sleep/Standby Modes**

As described in Power Requirements and Features of OMAP35x, the OMAP35x has many power management features that make it attractive in power-sensitive applications. One aspect of this is the sleep/standby modes of OMAP™3, which allow the device to enter very low power states while maintaining certain levels of functionality. The OMAP35x also has the ability to go into a deep sleep mode and still recognize wake-up events when needed.

With a TPS65023 power solution, you can implement a majority of these sleep/standby modes which allow you to take advantage of the power savings of an OMAP35x solution. Many different sleep/standby modes exist, depending on which portions of OMAP™3 need to be active for your application. With the TPS65023 solution, you have control over PLL and video DAC voltage, allowing you to completely shut off these supplies if needed. The MMC voltage can be controlled with an additional LDO if needed. (The TPS65023 has only one enable for both LDOs, so MMC and PLL both are either on or off at the same time.) You can also bring OMAP™3 into some sleep modes by reducing voltage on VDD_MPU_IVA to the lowest retention voltage (0.95 V). By implementing SmartReflex™ AVS, this voltage can potentially be lower, thus enabling further power savings. Using the PRCM (power reset control manager) in OMAP™3, you can also cut the power going to different domains on the device, including the domains for VDD_MPU_IVA and VDD_CORE. This brings you to near OFF mode power levels by reducing leakage power of OMAP™3.

The last step in OFF mode sequencing involves shutting down some voltage supplies. This step is supported by the TPS65023 power solution by using I2C writes to turn off and on the supplies. Note that only VDD_MPU_IVA voltage is adjustable (VDD_CORE is fixed). But you can still turn off these supplies to implement OFF mode.

Wakeup can then be achieved using I2C commands from the PRCM on OMAP™3. See the OMAP™3 TRM for more information on sleep and wakeup sequencing.

3.5  **Enabling Class-2 SmartReflex™ Implementations**

The TPS65023 power solution only supports Class-2 SmartReflex™ implementations. Class-3 SmartReflex™ implementation is not supported with this solution. However, with Class 2, you can achieve similar power savings as you can with Class 3.

**Class-2 SmartReflex Implementation**

With a Class-2 SmartReflex™ implementation, the ARM processor in OMAP™3 controls all of the functions of the TPS devices. You can use either OMAP3 I2C1, I2C2, or I2C3 to connect to the I2C port of the TPS65023. If possible, you must use a dedicated I2C bus between OMAP™3 and TPS65023. If you must share the bus with other peripherals, group the TPS65023 devices with peripherals which require only infrequent I2C activity. This avoids long latencies during voltage changes.

To configure the TPS65023 devices for Class-2 SmartReflex™ implementation, you must initialize them as follows:

- Set slew rate to either 7.2 or 14.4 mV/μs in DEFSLEW register (for OMAP™3, slew rate must be between 4-16 mV/μs).
- Control VDD_MPU_IVA voltage with DEFCORE register.
- Use LDO_CTRL to adjust LDO2 down to 3.15 if needed for MMC (OMAP™3’s nominal voltage is 3 V).
- After writing new voltage in DEFCORE, use GO bit in CON_CTRL2 register to change the voltage to the new value.

3.6  **MMC Boot**

The OMAP™3 processor has the ability to boot from many different sources. One possible boot configuration is to boot from MMC. This configuration requires that the MMC memory card is properly powered before ROM code executes (i.e., on power-on-reset).

If MMC boot is a requirement in your application, you must ensure that VDDS_MMC1 (and VDDS_MMC1A if using 8-bit MMC data) is set for 3-V operation at power up. It can later be turned off if necessary by your application.
In the TPS65023 power solution block diagram (Figure 3), the MMC voltage is connected to LDO2 of the TPS65023. The voltage is always enabled on power up, because it shares an enable signal with LDO1 (the source for OMAP™3 PLL voltage). If more control over MMC voltage is needed, you must use a discrete LDO to power OMAP™3 MMC voltage, and use OMAP™3 GPIOs to control its voltage and enable/disable signal. In the following example schematic (Figure 9), MMC1_EN and MMC1_VSET are connected directly to OMAP™3 GPIOs. To ensure this power device is enabled and supplying 3.15 V at OMAP3 power-on-reset, both MMC1_EN and MMC1_VSET must be high by default. To achieve this, choose OMAP™3 GPIOs, which default high at power up, or use an inverter where necessary.

Figure 9. LDO Circuitry to Provide MMC1 Voltage

Some applications can require MMC voltage sequencing to ensure 3.3 V is valid before 1.8 V. For this case, you can use two LDOs for each voltage to ensure proper sequencing, then enable/disable them using OMAP™3 GPIOs.
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