ABSTRACT

Unbuffered multiplexed ratio-metric analog-to-digital converters (ADC) have strict requirements on driving source impedance that are not always obvious. This application report addresses the trade-offs between source impedance and sample rate. It includes both 10-bit and 12-bit examples using the TMS570 and TMS470 family of processors in the GS30, GS40, and GS60 process nodes, i.e., F05/C05, F035/C035, and F021, respectively.

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1 Introduction

Unbuffered multiplexed ratio-metric ADCs are commonly used in microprocessors due to their simplicity of design and inherent absence of circuits that need trimming in production. Both multiplexed and unmultiplexed versions are commonly found in discrete form, and are probably the most common ADCs in existence. They have no internal buffer amplifiers to introduce input offset and gain errors, and no internal voltage references that might induce scaling errors.

Designers are accustomed to using these ADCs for a variety of low-frequency applications. Over the last two decades, they have been included in virtually every microprocessor family from every company and have increased in conversion speed right along with the microprocessors that host them.

A side effect of their advantages is that the sample capacitor within the ADC is directly charged by the external signal, and ever-increasing speed has made this a growing issue. While it may seem like a trivial problem to charge a 12 pF sample capacitor, at high conversion speeds it can be problematic to charge it to within 1/2 LSB in the allotted time.

Also, if the sample time is insufficient, then the charge left on the sample capacitor by the previous conversion of a channel can affect the accuracy of the channel currently being converted. This phenomenon is referred to as channel-to-channel crosstalk.

<table>
<thead>
<tr>
<th>Table 1. Terminology Used in This Document</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCLK</td>
</tr>
<tr>
<td>Channel Sample Frequency</td>
</tr>
<tr>
<td>Conversion Time</td>
</tr>
<tr>
<td>Group Conversion</td>
</tr>
<tr>
<td>Group-Cycle Time</td>
</tr>
<tr>
<td>VCLK</td>
</tr>
<tr>
<td>Offset Error</td>
</tr>
<tr>
<td>Sample Time</td>
</tr>
<tr>
<td>Settling Time</td>
</tr>
</tbody>
</table>

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2 System Model

Examine the overall environment in which the ADC is used. A model of the ADC system should include everything from the sensor or signal source to the ADC insides. Figure 1 partitions the system into four distinct blocks that are discussed individually.

**Figure 1. ADC System Model**

**Block 1:** The sensor can be virtually anything from a sophisticated mass air flow sensor to a brick striking a piezoelectric crystal. As such, the source voltage can range from microvolts (as from a thermocouple) to several thousand volts (the brick hitting a crystal). The source impedance and frequency can range similarly. With this in mind, not much is said about the source except that it clearly sets the requirements for the input of Block 2.

**Block 2:** This might best be described as a matching circuit. It has many simultaneous requirements to fulfill as noted in the figure.

It must maintain at least enough series resistance between the ESD entry point (if applicable) and the ADC input pin to protect the ADC's input from being damaged. For example, to pass the 4KV Contact Model ESD test, about 3000 Ω minimum resistance is required between the zap entry point and the ADC pin; most of the ADCs have 2KV ESD protection.

Any time something is digitized, it is essential that no information above the Nyquist frequency greater than a **no effect** level be introduced into the sampled signal. That means -67dB for 10 bits or -79dB for 12 bits. Once that noise is digitized, it is indistinguishable from the desired signal, so it had better be small. Therefore, the cutoff frequency of a low-pass filter (anti-aliasing filter) must be strategically positioned between the desired maximum signal frequency, f, and half of the input channel sampling frequency, fs/2 (Nyquist frequency). This filter is optional in some cases since some things just don't change very fast like the output of a thermistor, for example.

A level shifter is often required to match the peak signal level of the input to the nominal 3.3 V (or 5 V for some ADCs) swing of the ADC’s input to optimize the overall dynamic range. This circuit may be as simple as two resistors acting as a voltage divider, an active circuit like an opamp, or a sophisticated automatic gain control (AGC) circuit like that used with a variable reluctance speed sensor.

Impedance matching is often necessary to match a higher impedance sensor or level shifter to the requirements of Blocks 3 and 4. The impedance requirement of Blocks 3 and 4 for a given channel is dictated by the sampling frequency, fs, of that channel. While the previous three items in Block 2 are generally well understood by designers, the true requirements for source impedance to the ADC inputs are sometimes misunderstood. Understanding the ADC's source impedance requirements are the crux of this application report.

**Block 3:** This block is optional depending on required sampling speed, cost, and other factors. If it exists, it is simply a capacitor. It accumulates charge in continuous time, which can then be charge-shared with the ADC’s sample capacitor during the discrete-time sampling window of that channel.
3 ADC Input Model

Starting with Block 4, Figure 2 shows a simplified model of the input path of the TMSx70’s multiplexed unbuffered ADC.

There are two CMOS switches in the path between the ADIN[x] pin and the sample capacitor, Csamp. The first is an N-to-1 multiplexer that selects the channel to be converted; typically N = 16 or 32. The second is the sample-and-hold gate that is controlled by the ADC’s successive approximation state machine.

4 External Components

As mentioned previously with Blocks 2 and 3, it is common practice to add external components to the ADIN[x] pins that scale and filter the signal from the analog source. These components are determined by the requirements set by Blocks 1 and 4. A fairly typical circuit is shown in Figure 3.

Generally, most users place a large capacitor (Block 3) from the ADC pin to ground (Cext[x] shown in Figure 3). This capacitor is used to lower the source impedance of the channel as seen by the ADC so that the internal sample capacitor can be charged quickly. As noted earlier, this is a charge-sharing process between Cext and Cmux + Csamp (see Figure 2 and Figure 3), whose RC time constant is primarily determined by the maximum ADC input resistance (two switches with 250 Ω maximum each), the maximum multiplexer capacitance (16 pF) and maximum sample capacitance (13 or 22 pF) of the ADC.

In Figure 3, as Rsource is increased, the cutoff frequency created by Rsource and Cext is lowered. This means that the response time increases between when the sensor changes and when the change settles on Cext.
5 Symptoms of Inadequate Settling Time

Figure 4 through Figure 6 demonstrate the effect of having insufficient settling time for Csamp. For example, consider that there are two channels that you are converting in sequence within a 10 µS group-cycle time. The first channel has a 100 Hz square wave on it, and the second channel is a DC signal.

Figure 4 assumes the settling time is adequate for the chosen sample frequency. In other words, this is what you expect to see on the two ADIN pins when everything goes right:

![Figure 4. Adequate Settling Time](image)

Now reduce the allotted settling time (see Figure 5) so that the ADC only settles to within a few LSB rather than 1/2 LSB; these two signals are very low frequencies: 100 Hz and DC. Why should they have to settle?

![Figure 5. Insufficient Settling Time](image)

The top waveform has lost some bandwidth so the corners aren’t quite so square. But this may not be an issue if you are only interested in its minimum and maximum values.

However, the second waveform. ADIN\(_2\), has picked up crosstalk from the previous channel, ADIN\(_1\). If it was intended to be a DC level, this signal has been rendered just about useless. But what is the source of the problem?
The Effect of Cext

Zoom in, as indicated in Figure 5, on the lower trace’s rising edge, Figure 6.

![Figure 6. Close Examination of the Edges](image)

You should see a saw-tooth pattern that makes up the transition edge. In this example, the ratio of sample-frequency to signal-frequency is 1000:1, so there are probably a hundred or so steps rather than the dozen shown in Figure 6. As shown, the step spacing is at the channel cycle rate: 10 µS in this case. The vertical steps are caused by residual charge from the conversion of ADIN[1] left on Cmux and Csamp, creating a very small undesirable offset in Cext[1] during the conversion of ADIN[2]. The downward ramps are caused by the source for ADIN[2] attempting to recover the error via the source impedance of ADIN[2]. The difference between these two step-amounts is the error that accumulates on Cext[2] with time. As the error voltage across Rsourcing accumulates with each cycle, the step error becomes smaller and smaller until the vertical upward step and the downward ramp cancel each other.

On the oscilloscope, when zoomed out enough to see the 100 Hz waveform, the 100 KHz sampling artifacts of the crosstalk are completely invisible, and the basic exponential shape in Figure 6 looks like a clean square wave. In the general case, crosstalk looks like a vertically scaled image of ADIN[1] superimposed on ADIN[0].

6 The Effect of Cext

This section discusses Block 3 and the rationale for selecting Cext, or for that matter, even having Cext. To do this, SPICE is used to try several values of Cext and measure the time at which the voltage on Csamp settles to within 1/2 LSB of the exact value. For a 12-bit ADC at 3.3 V, this amounts to 403 µV. Plotting a curve of settling time versus Cext may tell us something about the nature of Cext.

Figure 7 shows a graph plotted from 39 runs of SPICE assuming two channels of the TMSx70 in continuous conversion mode. A mid-range value of 2000 Ω was chosen for Rsourcing.

The left-most point on the graph corresponds to Cext = 0 (but Cpad = 4 pF). As Cext is increased, it can be seen that the required settling time gets worse until Cext is around 200 nF. Then, there is a sharp roll-off in settling time until Cext is around 622 nF at which point the slope of the graph settles to near zero for further increases in Cext. This graph clearly illustrates that there is an optimum range for Cext. Section 8 shows how this optimum range is derived, but for now the shape of the curve needs to be understood in the graph shown in Figure 7 calculated for 12-bits.
For a 10-bit ADC, the curve will be similar but Cext values will be 4 times smaller assuming the same value for Csamp.

Figure 8 shows a hand-drawn time-domain plot of four SPICE runs on a 12-bit converter similar to Figure 7. This may help demonstrate the reason for the sudden drop in settling time as Cext increases; however, the waveforms have such huge scale differences that not even a log-log graph does an adequate job of placing them on the same plot, so there is some graphic license taken in Figure 8.
The object is to get Csamp charged to within 1/2 LSB of 3.3 V before declaring Csamp settled. Note that as Cext becomes much larger than Csamp, the curve looks more like two straight lines joined by a knee. As Cext gets larger, the knee gets sharper.

Below are the dependencies of each of the curves above:

(a)— With Cext = 0, there is effectively no discernible knee. The curve is a simple RC approximated by (Rsource + Rmux + Rsamp) * (Cmux + Csamp).

(b, c, d)—For the other three curves, charge-sharing jumps the voltage up to the knee with an RC time constant dominated by (Rmux + Rsamp) * (Cmux + Csamp). Then from the knee on, the RC time constant is dominated by Rsource * Cext.

(c, d)—As the knee rises above the \([3.3V - 1/2 \text{ LSB}]\) line with increasing Cext, there is a rapid reduction in time required for Csamp to settle since being within 1/2 LSB of the 3.3 V line is the definition of settled.

The vertical line segment is dominated by charge-sharing between Cext and (Cmux + Csamp). If, after charge-sharing, the knee falls short of the \([3.3V - 1/2 \text{ LSB}]\) line (Figure 8, curve B), then it can take a very long time to finish charging Cext and Csamp the rest of the way via Rsource. However, if the knee occurs at or above the line (Figure 8, curve C and D), then charging Csamp is already done, and all that remains is to complete the recharging of Cext. However, once Csamp is settled, the A-to-D conversion can proceed. Remember, there is a full group-cycle time to recharge Cext, which can be two orders of magnitude longer than a single channel’s cycle time.

7 Recharging Cext

During the charge-sharing process between Cext and [Cmux + Csamp], if you charge Cext by 1/2 LSB away from ideal, then in theory, you would have to wait an infinite amount of time for Cext to recover to its ideal value before you can attempt to charge-share again.

Try something more practical by waiting until Cext has recovered only to within 1/4 LSB before you charge-share again. Figure 9 shows that each successive charge-share pushes the error up until it settles in a range between 1/2 LSB and 1 LSB. This causes an effective 1 LSB of offset error in the voltage seen by the ADC.

![Figure 9. Recharging Cext](image-url)

Figure 9 and Figure 10, the vertical edges are due to charge-sharing with [Cmux + Csamp] while the downward sloped edges are due to Cext recovering via Rsource. The assumption here is that the previous channel was at 3.3 V and the current channel is at 0 V.
The term error here refers to the deviation in Cext’s voltage from ideal. The peak must never exceed 1/2 LSB to avoid crosstalk affecting the conversion result.

To solve this and improve offset error due to crosstalk, only allow Cext to charge to 1/4 LSB during charge-sharing. This can easily be accomplished by doubling the size of Cext relative to Figure 9. Also, recover Cext down to 1/8 LSB.

Now after several cycles, the time at which Cext begins charge-sharing with Csamp, i.e., the troughs, the error is only 1/4 LSB and the maximum error on Cext never exceeds 1/2 LSB at the peaks. This causes an effective 1/2 LSB of offset error in the voltage seen by the ADC.

8 Calculating Cext

This section discusses why Cext should be greater than or equal to about 622 nF for a 12-bit converter having Cmux = 16 pF and Csamp = 20 pF. To do this, the charge-sharing between Cext and Csamp needs to be examined. Note that Cmux + Csamp + tolerance (16 pF + (20 pF + 2 pF)) is used for charge-sharing calculations; ignore Cpad as it is tiny and in parallel with Cext.

First you need to develop the equation. Recalling that conservation of charge says something like “the total charge before sharing is equal to the total charge after sharing”:

\[
\text{before charge sharing, } \quad Q_{\text{samp}} = C_{\text{samp}} \times V_{\text{sam}} \quad \text{and} \quad Q_{\text{ext}} = C_{\text{ext}} \times V_{\text{ext}},
\]

\[
\text{conservation of charge, } Q_{\text{final}} = Q_{\text{amp}} + Q_{\text{ext}},
\]

\[
\text{capacitors in parallel add, } \quad C_{\text{total}} = C_{\text{samp}} + C_{\text{ext}},
\]

\[
Q_{\text{final}} = C_{\text{total}} \times V_{\text{final}},
\]

\[
\text{substituting [1], [2] and [3] into [4], } \quad (Q_{\text{ext}} + Q_{\text{amp}}) = (C_{\text{ext}} + C_{\text{samp}}) \times V_{\text{final}}
\]

\[
\text{solving for } V_{\text{final}}, \quad V_{\text{final}} = \frac{Q_{\text{ext}} + Q_{\text{amp}}}{C_{\text{ext}} + C_{\text{samp}}}
\]
Calculating Cext

substituting [1] into [6],

\[
V_{\text{final}} = \frac{(C_{\text{ext}} \cdot V_{\text{ext}} + C_{\text{amp}} \cdot V_{\text{amp}})}{(C_{\text{ext}} + C_{\text{amp}})}.
\]  

(7)

where \(V_{\text{final}}\) is the voltage remaining on \(C_{\text{ext}}\) after charge-sharing with \(C_{\text{amp}}\).

It can be seen that for a 12-bit ADC settling to within 1/2 LSB, \(V_{\text{final}}\) would have to be:

\[
V_{\text{final}} = \left( \frac{\text{Vin}}{2^{(12 + 1)}} \right) - 0.999878 \times \text{Vin}
\]

(8)

where \(\text{Vin}\) is the desired input signal value.

Now, recall that it was concluded earlier that you actually have to settle \(C_{\text{amp}}\) to within 1/4 LSB to allow room to keep \(C_{\text{ext}}\)’s worst-case error below 1/2 LSB; therefore,

\[
V_{\text{final}} = \left( \frac{\text{Vin}}{2^{(10 + 1 + 1)}} \right) - 0.999939 \times \text{Vin}
\]

(9)

In a nominal 3.3 V system, this amounts to a worst-case value of 201 µV.

For a 10-bit ADC settling to within 1/4 LSB, \(V_{\text{final}}\) would have to be:

\[
V_{\text{final}} = \left( \frac{\text{Vin}}{2^{(10 + 1 + 1)}} \right) - 0.999756 \times \text{Vin}
\]

(10)

and in a nominal 3.3 V system, this amounts to 403 µV.

Assume now that \(C_{\text{amp}}\) is discharged, \(C_{\text{ext}}\) holds the value \(\text{Vin}\), and \(V_{\text{final}}\) must end up at 0.999939 \times \(\text{Vin}\) (that is, to within 1/4 LSB of \(\text{Vin}\) @ 12 bits) from equations [7] and [8],

\[
\text{Vin} \times \left( \frac{1}{2^{(12 + 2)}} \right) = \frac{(C_{\text{ext}} \cdot \text{Vin} + C_{\text{amp}} \cdot 0)}{(C_{\text{ext}} + C_{\text{amp}})}
\]

(11)

\[
(C_{\text{ext}} + C_{\text{amp}}) \times \left( \frac{1}{16384} \right) = C_{\text{ext}}
\]

(12)

solving for \(C_{\text{ext}}\),

\[
C_{\text{ext}} = 16383 \times C_{\text{amp}}
\]

(13)

for a 12-bit converter with \(C_{\text{mux}} = 16 \text{ pF}\) and \(C_{\text{amp}} = 20 \text{ pF}\),

\[
C_{\text{ext}} = 16383 \times (16 + 20 + 2) \text{pF} = 622 \text{nF}
\]

(14)

for a 12-bit converter with \(C_{\text{mux}} = 16 \text{ pF}\) and \(C_{\text{amp}} = 12 \text{ pF}\),

\[
C_{\text{ext}} = 16383 \times (16 + 12 + 1) \text{pF} = 475 \text{nF}
\]

(15)

for a 10-bit converter with \(C_{\text{mux}} = 16 \text{ pF}\) and \(C_{\text{amp}} = 20 \text{ pF}\),

\[
C_{\text{ext}} = 4095 \times (16 + 20 + 1) \text{pF} = 156 \text{nF}
\]

(16)

for a 10-bit converter with \(C_{\text{mux}} = 16 \text{ pF}\) and \(C_{\text{amp}} = 12 \text{ pF}\),

\[
C_{\text{ext}} = 4095 \times (16 + 12 + 1) \text{pF} = 119 \text{nF}
\]

(17)
Calculating \( R_{source} \)

This is an absolute minimum value of \( C_{ext} \). Be sure when picking its value to include tolerance and aging factors. Larger values are fine but have practically no effect on sample time and only limited effect on group-cycle time. This is discussed in more detail later.

Assuming a 12-bit ADC, having \( C_{ext} < 16383 \times C_{samp} \), requires that \( C_{samp} \) be charged entirely during the sample time rather than during the group-cycle time. So \( C_{ext} < 16383 \times C_{samp} \) is essentially a different mode of operation from \( C_{ext} > 16383 \times C_{samp} \).

From the standpoint of speed and \( R_{source} \) requirements, you are actually better off with no external cap if \( C_{ext} < 16383 \times C_{samp} \), assuming there is no anti-aliasing filter. This was shown dramatically in the previous graphs.

### 9 Calculating \( R_{source} \)

The total resistance feeding the external capacitor, \( C_{ext} \), is called \( R_{source} \). Namely, it is the Thevenin equivalent resistance of the driving source as viewed by \( C_{ext} \).

![Figure 11. Thevenin Equivalent Model](image)

The time constant required for an RC circuit to settle to within 1/4 LSB with 12 bits of resolution is:

\[
\tau = \ln \left( 2^{(12 + 2)} \right) = 9.7 \text{ time constants}
\]

(18)

For 10 bits,

\[
\tau = \ln \left( 2^{(10 + 2)} \right) = 8.3 \text{ time constants}
\]

(19)

Given a group-cycle time, \( T_{cyc} \), the value of \( R_{source} \) required to replenish the charge depleted from \( C_{ext} \) is given by the relationship:

\[
R_{source} < \frac{T_{cyc}}{\tau \times C_{ext}}
\]

(20)

But rather than do a lot of calculations, a table developed from a lot of SPICE runs is much easier, and the calculation of ADC settling time gets messy due to the ADC having two closely spaced poles (see Section 3).
Table 2 shows settling times for different types of ADCs versus source impedance. To use this table, find your ADC in the first 3 columns based on data sheet specs. Secondly, if you use an external capacitor, Cext, make sure it is as big as the one listed in the 4th column after accounting for tolerance and aging. If your Cext is larger than the one listed, it will affect the result columns favorably, if at all.

### Table 2. Settling Time vs. Source Impedance

<table>
<thead>
<tr>
<th>ADC Channels</th>
<th>ADC Res, Bits</th>
<th>Datasheet Csamp, pF</th>
<th>Minimum Cext, nF</th>
<th>Rsource, Ω</th>
<th>Csamp Settling to 1/2 LSB, nS</th>
<th>Cext Recovery to 1/4 LSB, µS</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>10</td>
<td>20 ± 2</td>
<td>0</td>
<td>200</td>
<td>159</td>
<td>15 µS</td>
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<tr>
<td>16</td>
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<td>20 ± 2</td>
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<td>16</td>
<td>12</td>
<td>12 ± 1</td>
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<td>68 µS</td>
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<tr>
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<td>475</td>
<td>2K</td>
<td>89</td>
<td>682 µS</td>
</tr>
</tbody>
</table>

Note from the table that settling time of Csamp becomes independent of source impedance if Cext is at least the minimum value previously calculated.

Next, looking at the settling time of Cext, the effects of varying Rsource are quite linear so you can easily interpolate using your timing requirements to obtain the required source resistance.

Using an example of Table 2, keep in mind that the entire group-cycle time is used to recover Cext. Assume you have a 16-channel 10-bit ADC whose listed sample cap is 20 pF. You have a group of channels that must be converted every 15 µS. Using the data in the forth line of the table, if an Rsource of 200 Ω yields a 21 µS recovery time for Cext, i.e., group-cycle time, then using linear interpolation, a 15 µs recovery time would require an Rsource of:

$$R_{source} < \frac{200 \times 15}{21} = 143 \Omega$$

(21)

You can see from this example that to speed up the recovery of Cext from 21 µS to 15 µS, it is necessary to reduce source impedance from 200 Ω to 143 Ω or less.

Note that if you, for example, double the size of Cext beyond the value in Table 2, it is not necessary to recalculate anything, just interpolate as if you had used the exact value of Cext listed in the table. Either way, the same amount of charge is removed/recovered.
Consequences of Inadequate Settling Time

If $C_{ext}$ is at least as large as what is shown in Table 2, then the maximum time to settle $C_{samp}$ is less than 130 nS, which is very small. There should never be a need to cheat on this parameter.

The only time it makes sense to omit $C_{ext}$ is when $R_{source}$ is very low, otherwise, the channel will be sensitive to noise. Generally, $R_{source}$ is low only with sensors that have outputs driven by opamps. In this case, $R_{source}$ is < $100 \Omega$ and still there is no need to cheat on settling time.

Inadequate settling time leads to crosstalk. As discussed at the beginning of this document, this is charge transferred from one channel to the next and accumulated on $C_{ext}$ over many conversion cycles. With crosstalk, each channel disturbs the next channel in the group to be converted. This phenomenon is due to the residue of charge on $C_{samp}$ after converting channel$_{[N]}$, which contaminates the charge on $C_{ext}$$_{[X+1]}$ of channel$_{[X+1]}$.

A very good rule is don’t cheat on settling time.

Consequences of High Source Impedance

If $R_{source}$ is too high for the desired conversion time, the only consequence is a time lag in the response of the channel. Full 1/2 LSB accuracy will occur, but it will be delayed according to [18] and [19].

If $C_{ext}$ is not present or if it is too small and you have cheated on settling time, then results will be inaccurate; there will be crosstalk and full 1/2 LSB will never occur.

A very good rule is don’t cheat on settling time.

Solutions

For those of you who insist on cheating, there is a software-selectable feature that is included on newer TMSx70 ADCs that allows the application to discharge $C_{samp}$ between conversions. The minimum time required to perform this discharging process is typically about 1 to 2 ADC clock cycles.

Using this feature is not a panacea. If you use it and cheat on settling time, it will provide a result that is scaled from the actual value. This scaled value is predictable only if the group-cycle time and channel-to-channel timing are well behaved. If the timing varies, the scaling factor will vary as well.

The only reason to use this discharge feature is to reduce the cost of using the correct value for $C_{ext}$; however, it can be used successfully if ADC timing is well behaved.

Conclusions

Unbuffered multiplexed ratio-metric ADCs are excellent in terms of cost and producibility, but careful consideration must be used in designing in order to obtain the expected results.

Most notable are the following points:

- Settling time issues can be easily diagnosed by examining the waveforms at the ADIN$_{[X]}$ pins while the ADC is running in a continuous loop.
- In most cases, the best speed/impedance results are obtained by including $C_{ext}$ if the proper value is selected.
- Given a specified number of bits of resolution, the proper value of $C_{ext}$ can be calculated independent of frequency and source impedance.
- Never cheat on settling time. It only provides you with unpredictable results.
- If you do cheat, use the Discharge feature and continuous Group Conversion; expect scaled results.

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- Advanced CMOS Logic Data Book”, Texas Instruments, 1993, SCAD001C
- Choosing an Anti-Alias Filter, Steve Hendrix, January 2001
- CoreSight and Trace for Cortex-R Series Processors http://www.arm.com/products/system-ip/debug-trace/coresight-for-cortex-r.php
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