Introduction
With the optimal combination of the TMS320C6412 DSP and TMS320C6416 DSP Starter Kit (DSK), designers can lower overall system cost in their high-performance design.

With clock rates at 500 and 600 MHz, the C6412 DSP enables designers to increase system performance while reducing overall system cost through its combination of low-price point, high-frequency performance, integrated peripherals, large on-chip memory and more channels per processor.

The new C6416 DSK (part number TMDSDSK6416) provides an easy-to-use, cost-effective development tool, allowing designers to evaluate the C6412 DSP in their high-performance design.

Lower system cost: The performance factor
The C6412 DSP is available at two clock rates: the 600-MHz device offers performance up to 4800 MIPS and the 500-MHz device provides performance up to 4000 MIPS. With many on-chip peripherals, the C6412 DSP offers a cost-effective, high-performance DSP to meet programming challenges. The C6412 DSP provides the operational flexibility of high-speed controllers and the numerical capability of various processors.

The C6412 DSP is a code-compatible member of the TMS320C6000™ DSP platform, the highest-performance, fixed-point DSP generation. Based on TI’s second-generation high-performance, advanced VelociTI.2™ very-long-instruction-word (VLIW) architecture, the C6412 DSP is an ideal device for high-end networked applications.

The C6412 DSP uses a two-level cache-based architecture that increases performance and reduces system cost. Cache memories greatly reduce the CPU-to-memory processing bottleneck. Caches are small, fast memory residing between the CPU and (slower) system memory. The cache provides code and data to the CPU at the speed of the processor while automatically managing the data movement from the slower main memory, which is frequently located off-chip. The Level 1 program cache (L1P) is a 128-Kbit direct-mapped cache, while the Level 1 data cache (L1D) is a 128-Kbit
two-way set-associative cache. The Level 2 memory/cache (L2) consists of a 2-Mbit memory space shared between program and data space. L2 memory can be configured as mapped memory, cache or combinations of the two.

**Architecturally designed for performance**

The TMS320C6412 DSP core processor has 64 general-purpose registers of 32-bit word length and eight highly independent functional units—two multipliers for a 32-bit result and six arithmetic logic units (ALUs)—with VelociTI.2™ extensions.

The VelociTI.2 extensions in the eight functional units include new instructions to accelerate performance in applications and extend the parallelism of the VelociTI™ architecture. The C6412 DSP produces four 32-bit multiply accumulates (MACs) per cycle for a total of 2400 million MACS (MMACS) or eight 8-bit MACs per cycle for a total of 4800 MMACS. The C6412 DSP also provides application-specific hardware logic, on-chip memory and additional on-chip peripherals similar to other TMS320C6000™ DSP platform devices.

**Economizing board space and reduced bill of materials**

Designers using the C6412 DSP experience substantial savings on a system’s bill of materials (BOM) cost as the C6412 DSP increases channel density while maintaining low system cost. These cost savings are delivered without sacrificing the ability to customize and differentiate application functionality.

The C6412 DSP’s large on-chip memory reduces the need for external memory, saves board space and provides performance advantages over systems that require off-chip memory accesses.

The C6412 DSP reduces the number of necessary on-board components due to its high degree of on-chip peripheral integration. Its peripheral set includes a 10-/100-Mb/sec Ethernet Media Access Controller (EMAC); a Management Data Input/Output (MDIO) module; an Inter-Integrated Circuit (I²C) bus module; two Multi-channel Buffered Serial Ports (McBSPs); three 32-bit general-purpose timers; a user-configurable 16-bit or 32-bit Host Port Interface (HPI16/HPI32); a Peripheral Component Interconnect (PCI); a 16-pin general-purpose input/output port (GP0) with programmable interrupt/event generation modes and a 64-bit glueless External Memory Interface (EMIF) capable of interfacing to synchronous and asynchronous memories and peripherals.
Reduced manufacturing costs

**EMAC**
The EMAC provides an efficient interface between the TMS320C6412 DSP core processor and the network. The C6412 DSP EMAC supports 10Base-T and 100Base-TX or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex with hardware flow control and quality of service (QoS) support. The C6412 DSP EMAC uses a custom interface to the DSP core that allows efficient data transmission and reception, supporting high-speed, high-bandwidth throughput between the network and the DSP. The advantage of the C6412 DSP’s on-chip, highly integrated peripherals such as the EMAC is illustrated in a networked application environment such as VoIP. Earlier DSP-based VoIP system implementations without EMAC required the DSP to be connected to the Ethernet backplane via glue logic (or FPGA). The C6412 DSP’s on-chip EMAC allows direct DSP connection to the Ethernet backplane, eliminating the FPGA and lowering system cost.

**HPI**
A 32-bit wide HPI provides dedicated connection to a variety of industry-standard host processors and PCI bridge chips. The HPI can operate in either a 32-bit (HPI32) or 16-bit (HPI16) wide mode. The HPI also can be used as a slave port where a mastering peripheral can stream data to the DSP. Through the HPI, the host controller has access to the DSP’s entire memory map and also can access memory-mapped peripherals through the host interface.

**PCI**
The C6412 DSP features a 32-bit address/data bus at 66 MHz. It contains the logic required to implement a fully compliant PCI specification revision 2.2 bursting master/slave with access to the DSP’s memory map (peripherals, on-chip RAM and external memory) through the EMIF. This architecture allows both PCI master and slave transactions, while keeping the enhanced DMA (EDMA) channel resources available for additional applications.

**Reduced manufacturing costs**
The C6412 DSP is available in two 548-Ball Grid Array (BGA) package sizes: 23 mm (GDK) and 27 mm (GNZ). The 23-mm package is ideal for customers concerned with saving board space and offers a 0.8-mm ball pitch. Since the 1-mm pitch provides increased clearance for spaces and traces, the 27-mm package permits the use of less expensive printed circuit board technology. This is due to the 1-mm pitch providing increased clearance for spaces and traces. The 1-mm BGA pitch also increases the available universe of board assembly vendors, as many may not have migrated their systems to support 0.8-mm board pitches.
Development tools that reduce time-to-market

The TMS320C6416 DSK offers designers an easy and low-cost method to evaluate the high-performance TMS320C6412 DSP designs.

Developed jointly with Spectrum Digital, the kit uses USB communications for true plug-and-play functionality. Experienced and novice designers can design innovative products immediately with the DSK’s Code Composer Studio™ (CCStudio) v2.2 integrated development environment (IDE) and eXpressDSP™ software that includes DSP/BIOS™ kernel and Reference Frameworks.

The C6416 DSK tools include the latest fast simulators from TI and access to the Analysis Toolkit via Update Advisor that features the Cache Analysis tool and Multi-Event Profiler. Using Cache Analysis, developers can improve the performance of their application by providing a graphical view of the on-chip cache activity. Over time, designers can quickly determine if a block of code is using the on-chip cache to achieve peak performance.

The C6416 DSK enables designers to download and move through code quickly and uses Real-Time Data Exchange (RTDX™) for improved host and target communications.

The DSK features the C6416 DSP, a 600-MHz device delivering up to 4800 MIPS and designed to meet the needs of high-performing, memory-intensive applications such as networking, video, imaging and most multi-channel systems. Other hardware features of the C6416 DSK board include:

- Embedded JTAG support via USB
- A high-quality 24-bit stereo codec
- Four 3.5-mm audio jacks for microphone, line in, speaker and line out
- 512 Kwords of Flash and 16 MB of SDRAM
- An expansion port connector for plug-in modules
- An on-board standard IEEE JTAG interface
- A +5-V universal power supply

Designers can readily target the C6416 DSP through TI's CCStudio DSK development platform. The tools run on Windows® 98, 2000 and XP and allow developers to seamlessly manage projects of varying complexity.
Conclusion
Through its combination of low-price point, high-frequency performance, integrated peripherals, large on-chip memory and more channels per processor, the C6412 DSP enables system designers to increase system performance while reducing overall system cost. TI’s new TMS320C6416 DSK provides designers an easy-to-use, cost-effective way to take their high-performance TMS320C64x™ DSP generation designs from conception to production.

The TMS320C6412 DSP also offers a range of peripherals making it a fit for networked applications such as voice-over-packet and network security cameras. With the C6412 DSP, networking applications designers can achieve increased system performance, lower system cost to their end customer and increased channels per processor over their existing generation of devices.
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