**Introduction**

In today’s increasingly complex and interconnected world, system-on-a-chip (SoC) performance requirements are influenced by existing as well as evolving and emerging applications. Continued consolidation of the functionality required to meet performance and cost targets has led Texas Instruments (TI) to re-examine many of the basic building blocks of existing SoC solutions.

TI’s new multicore, multilayer SoC architecture will power a family of devices targeted at advanced communications infrastructure applications, such as those found in carrier networks and wireless base stations. These devices are based on a flexible and comprehensive multicore architecture and incorporate a software ecosystem that eases programming burdens while providing industry-leading performance and shortened development time.

**Multicore, multilayer SoC architecture**

SoC is a concept that has been around for a long time; the basic approach is to integrate more and more functionality into a given device. This integration can take the form of either hardware or solution software. Performance gains are traditionally achieved by increased clock rates and more advanced process nodes. Many SoC designs pair a DSP with a RISC processor to target specific applications.

A more recent approach to increasing performance has been to create multicore devices. In this scenario, it’s important to manage the competition for processing resources so that the full entitlement of the device can be realized. TI’s new multicore, multilayer SoC architecture addresses these challenges and creates the first true network-on-chip infrastructure to unleash full multicore entitlement.

**Advancing Moore’s Law**

The move to more advanced process nodes has been a key driver in keeping up with Moore’s Law. In the case of TI’s new family of devices, a move to 40 nanometers provides an impressive performance boost – but today’s applications require more.

TI’s new SoC architecture provides the flexibility to include targeted coprocessing, fixed- and floating-point operation, optimized inter-element communication, and a variety of processor types (DSP, VSP, ARM®, etc.). TI’s architecture incorporates DSP cores capable of both 32 GMACs per core for fixed-point operations and 16 GFLOPS for floating-point operations. This represents a performance boost that far exceeds the expectation of Moore’s Law in a single generation and also brings to market the first floating-point processor capable of operating at the highest DSP performance levels. Figure 1 on the following page illustrates the new architecture.
TI has designed comprehensive connectivity planes — TeraNet 2 which provides throughput of 2 terabits per second — to address the need to seamlessly interconnect various processing elements. TI’s Multicore Shared Memory Controller provides direct access to the on-chip shared memory system and external DDR3 memory without robbing internal switch-fabric bandwidth, while TI’s Multicore Navigator facilitates and manages communications across the SoC architecture through more than eight-thousand elements. HyperLink 50 allows the interconnection of companion devices such as additional coprocessors or companion TI SoCs.

**Simplifying the software ecosystem**

With all of the advances made in multicore, multilayer SoC architectures, TI has taken bold steps to enable an efficient, simplified software development ecosystem to provide full silicon entitlement to application developers. The resulting ecosystem targets all SoC components shown in Figure 2 and is summarized as:

- Support for various peripherals (PCIe, SRIO, Ethernet)
- Management of coprocessors
- Enabled connectivity within each device
- Multiple operating systems preintegrated with drivers, coprocessors and connectivity software (Linux, DSP/BIOS™ real-time kernel)
- The industry’s most efficient toolkit
Texas Instruments

Realizing full multicore entitlement

February 2010

TI recognizes that existing and emerging applications will demand different uses for the multiple layers and processing elements/cores. Some applications may use each core independently; others may want to use one processing element as master while other processing elements are designated slaves. In a third variant, all processing elements could be peers, and tasks are dynamically allocated. Some applications might want to use the device as a high-performance compute (HPC) engine enabled through such standards as OpenCL and OpenMP.

To provide such diverse application development, TI will offer a basic enabler software development toolkit that encompasses the enabler software, tools and operating system for application developers. This toolkit has been developed in lockstep with the silicon advances to ensure optimized access to various accelerators and multilayer connectivity planes for application developers.

TI has worked very closely with its software development partners to ensure that the tools, software and operating systems will use the architecture features seamlessly.

A strong software ecosystem is the basis in the development of successful multicore solutions. With TI’s enabler software and tools, along with a rich offering from TI’s software partners, the power of TI’s multicore, multilayer silicon architecture is now open to

Flexible and broad approach to software

Achieving network-on-chip capabilities

Figure 2. Multicore, multilayer software ecosystem
customers, enabling them to develop exciting new applications for today’s and tomorrow’s connected world.

Based on the new SoC architecture, TI’s new family of devices is a large step forward in enabling more comprehensive network-on-chip capability. As TI continues to invest in multicore technologies, the new SoC architecture will provide a basis for roadmap development and a solid foundation for future customer development.

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